Cpr E 281 HW 12

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Fifteenth Week
Due Date: Dec. 4, 2017

P1. (15 points) A sequential circuit has 2 rising edge triggered flip-flops (outputs A and B), two inputs (X and Y) and one output Z. One of the flip-flops is D the other is JK. The logic expressions for this circuit are:

$$\begin{aligned} D_a &= X' \cdot Y + X \cdot A \\ J_b &= X' \cdot B + X' \cdot A \\ K_b &= Y \cdot B \\ Z &= X \cdot B \end{aligned}$$

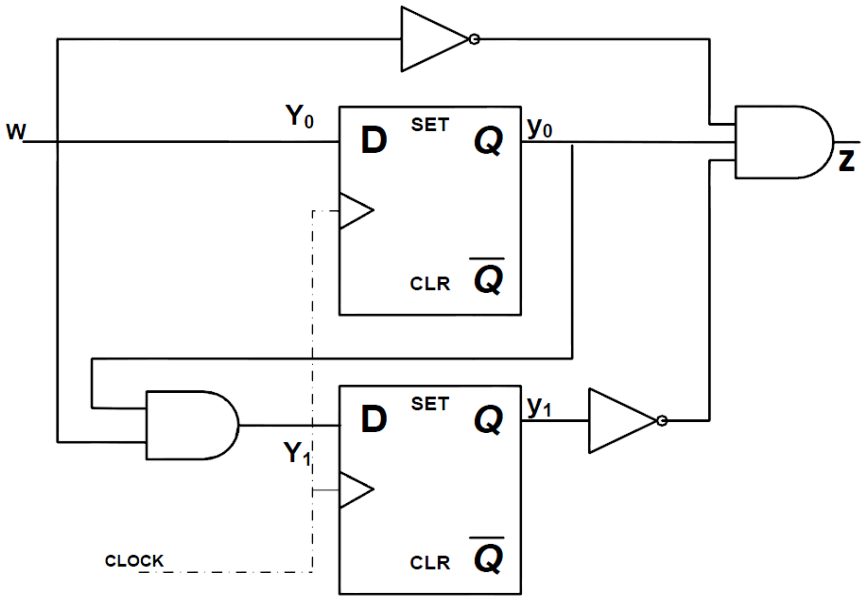
a) Sketch the circuit diagram
b) Construct the transition table
c) Construct the state diagram

P2. (40 points) A counter has a special counting sequence: 0, 5, 7, 1, 0, 5, 7, 1, and so on. Design this counter with minimal number of states.

a) (5 points) Draw the state diagram for the counter.
b) (5 points) Construct the state-assigned table including the next state and output.
c) (10 points) Draw the circuit diagram for the counter using D flip-flops.
d) (10 points) Repeat (c) using T flip-flops.
e) (10 points) Repeat (c) using JK flip-flops.

P3. (15 points) Use synchronous sequential circuit (SSC) analysis to reverse engineer the operation of the circuit shown below.

a) Is this a Mealy or Moore machine?
b) Write the expressions for Next State and Output logic.
c) Draw the state transition diagram.



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P4. (10 points) Draw the state diagram for a Mealy state machine with two inputs (X and Y) and two outputs (Z1 and Z2). The two inputs represent a two-bit binary number (N). If the present value of N is greater than the previous value of N then Z1=0 and Z2=1. And if the present value of N is less than the previous value of N then Z1=1 and Z2=0. Otherwise Z1=Z2=0.

P5. (20 points) Convert each of the following FSMs (shown below) to an ASM chart.