Cpr E 281 HW 11

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Fourteenth Week
Due Date: Nov. 27, 2017

P1. (10 points) Draw a state transition diagram for:

(a) A state machine that reads in a sequence of binary digits, one at a time, and stops when it has read in a total of five 1s (need not be consecutive). To "stop" the machine, merely have it loop repeatedly in a final state.

(b) A state machine that stops when it has read in at least three consecutive 1s followed by a 0.

P2. (15 points) Design a three-bit counter-like circuit controlled by the input w. If w=0, then the counter subtracts 1 from its contents (acting like a normal down-counter). If w=1, then the counter adds 2 to its contents, wrapping around if the count has to become 8 or 9. Thus if the current state is 6 (or 7) and w=1, then the next state is 0 (or 1). Use D flip-flops in your circuit. Let y_2, y_1, and y_0 be the current state values.

(a) Draw a state diagram for the machine.

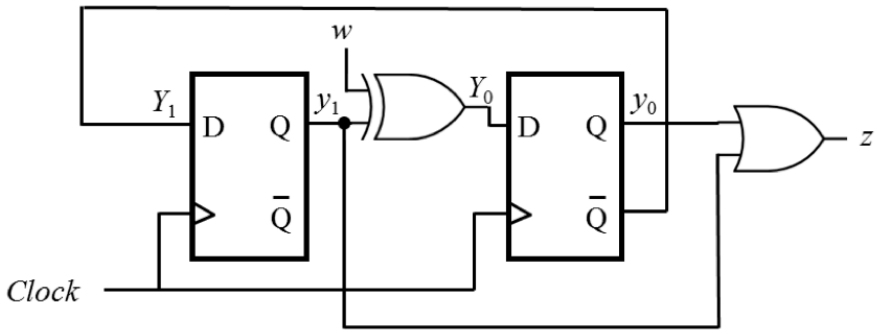
(b) Construct a state assignment table including the next state and output.

(c) Write the simplified expressions for the next state and output logic.

P3. (10 points) Repeat P2 using T flip-flops in your circuit.

P4. (10 points) Derive a minimal state table for a single-input and single-output Moore-type FSM that produces an output of 1 if in the input sequence it detects either 110 or 101 patterns. Overlapping sequences should be detected. Repeat this problem for a Mealy-type FSM.

P5. (15 points) A FSM has two D flip-flops, an input *w*, and an output *z*. The circuit diagram is shown below.



a) (5 points) Find the logic expressions of Y_1, Y_0, and the output *z*.

b) (5 points) Show the state-assigned table of the FSM.

c) (5 points) Draw the state diagram of the FSM.

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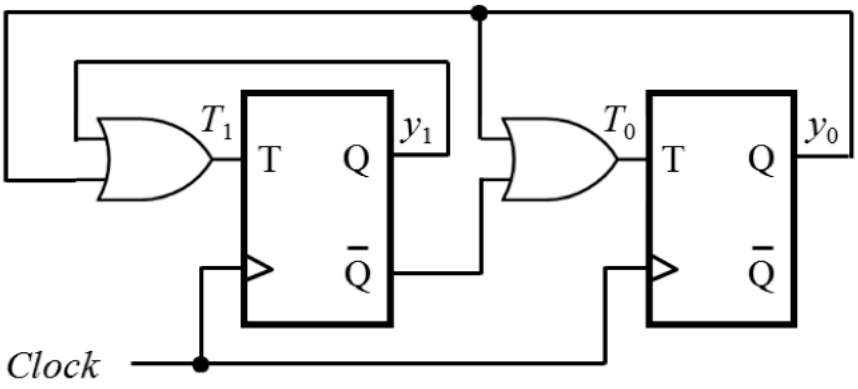
P6. (10 points) A two-bit counter has the following circuit diagram. The output is $z_1z_0 = y_1y_0$.



a) (5 points) Draw the state diagram of the counter.
b) (5 points) What is the repeated counting sequence of this counter?

P7. (20 points) Consider the following state table for a FSM.

Present State	Next State		Output
	w=0	w=1	z
A	A	B	0
B	B	C	1
C	C	D	0
D	D	A	1

a) (5 points) Draw the state diagram of the FSM.
b) (3 points) Draw the circuit diagram of the FSM using D flip-flops.
c) (3 points) Perform state minimization to minimize the number of states. Show your partitions in the procedure.
d) (3 points) Draw the new state diagram of the minimized FSM.
e) (3 points) Draw the circuit diagram of the minimized FSM using D flip-flops.
f) (3 points) Compare the circuits in (b) and (e), what is the benefit of state minimization?

P8. (10 points) The arbiter FSM defined in section 8.8 (Figure 8.72) may cause device 3 to never get serviced if devices 1 and 2 continuously keep raising requests, so that in the Idle state it always happens that either device 1 or device 2 has an outstanding request. Modify the proposed FSM to ensure that device 3 will get serviced in that situation. That is, if it raises a request, then devices 1 and 2 will be serviced only once before device 3 is granted its request.