Cpr E 281 HW 09
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Registers and Counters
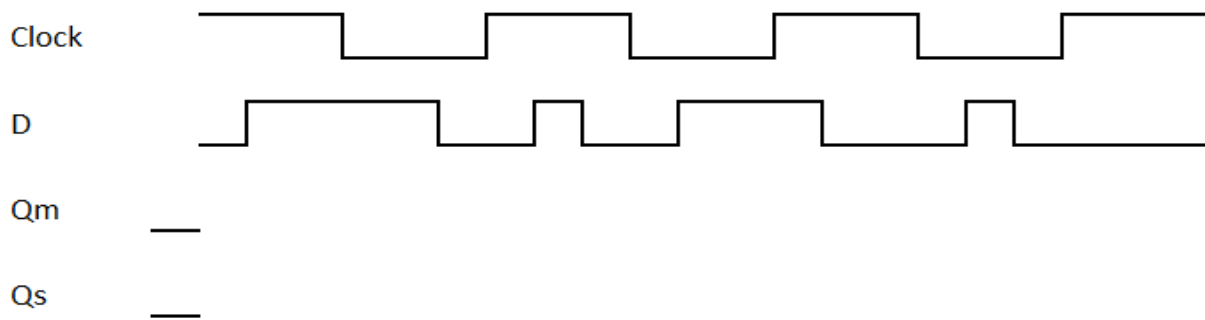## Assigned Date: Eleventh Week
Due Date: Nov. 6, 2017

P1. (10 points) Consider a positive-edge triggered master-slave D flip-flop design. For the input Clock and D given below, complete the timing diagram for Qm and Qs. Then briefly explain why this flip-flop design is positive-edge triggered.


P2. (10 points) Complete the timing diagram for Q for a negative edge triggered JK flip-flop, given the following values of the clock C and the inputs J and K.
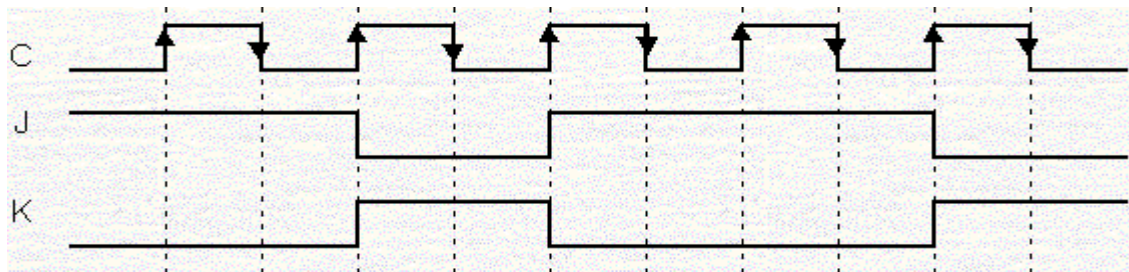
P3. (20 points) Design a 4-bit register with both shift and parallel load features. The inputs of the register include a 2-bit control code X Y, a 4-bit input value I3 I2 I1 I0, and a clock signal. The outputs of the register are the 4 bits Q3 Q2 Q1 Q0 that represent the value stored in the register. You are allowed to use any number of D flip-flops, multiplexers of any size, decoders and encoders of any size, AND gates, OR gates, and NOT gates. (Notice that you do not need all of them.) The four operations of the register are defined below:

X Y	Operation
0 0	Hold the current value stored (i.e., Q3 Q2 Q1 Q0 are not changed)
0 1	Shift right (i.e., new Q3=I3, new Q2=Q3, new Q1=Q2, new Q0=Q1)
1 0	Shift left (i.e., new Q3=Q2, new Q2=Q1, new Q1=Q0, new Q0=I0)
1 1	Load new data (i.e., new Q3=I3, new Q2=I2, new Q1=I1, new Q0=I0)

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P4. (10 points) Complete the following timing diagram for Q_a, Q_b, and Q_c, which are the outputs of a gated D latch, a positive-edge-triggered D flip-flop, and a negative-edge-triggered D flip-flop. Assume that $Q = 0$ initially anxd no gate delays. (5 points each).
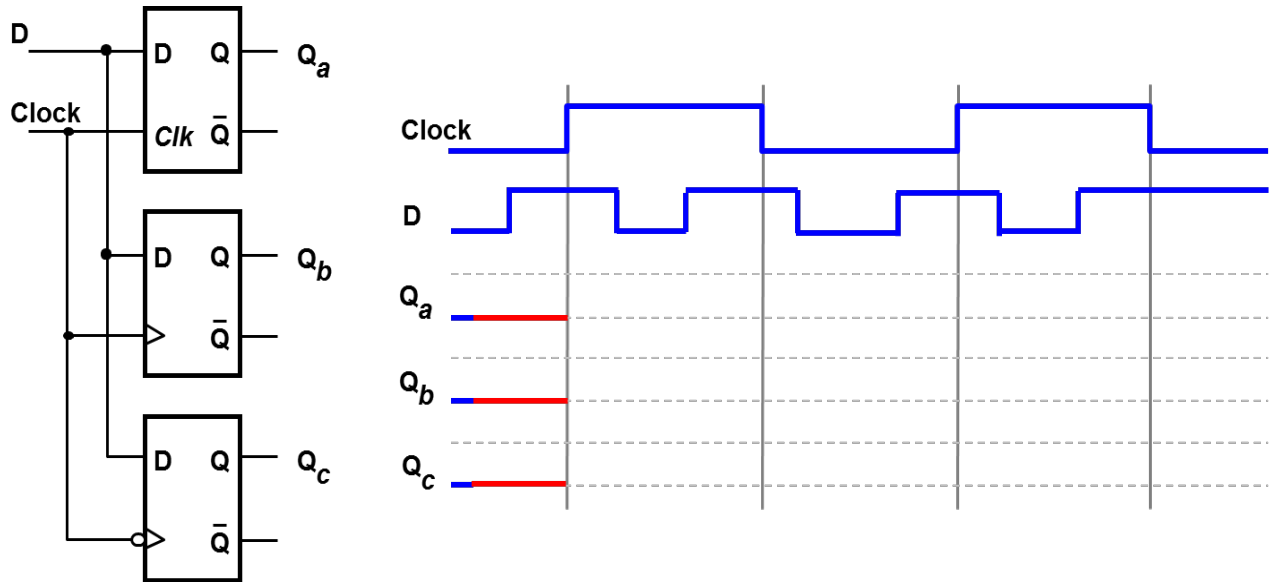
P5. (10 points) Construct a JK flip-flop using a T flip-flop.

a) Complete the following truth table.

| J | K | Output | | T |
		Q(t)	Q(t+1)	
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

b) Write down the simplified SOP expression of T using J, K, and Q(t) for inputs.

c) Draw the circuit for a JK flip-flop using a T flip-flop and other necessary gates. Make sure that you connect the flip-flop to a clock signal.

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P6. (15 points) For each of the following three cases, follow the three steps in P5 to:
    (a) Construct a D flip-flop using a JK flip flop.
    (b) Construct a D flip-flop using a T flip flop.
    (c) Construct a T flip-flop using a JK flip flop.

P7. (5 points) The circuit below looks like a counter. What is the sequence that this circuit counts-in?
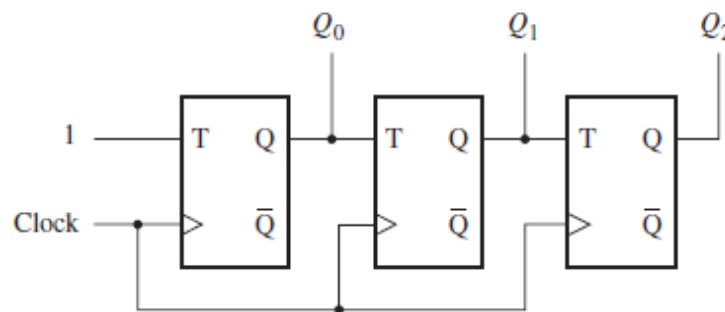
P8. (10 points) Design a 4-bit asynchronous up/down-counter with Enable using T flip-flops and any combinational circuit devices. The direction of the counter is controlled by a 1-bit signal U. If U=1, the counter will count up. If U=0, the counter will count down. The counting can be enabled/disabled by a 1-bit signal E. If E=1, then the counter will count on the positive clock edge. If E=0, then the counter will keep the same value stored.

P9. (10 points) Design a shifter circuit that can shift a four-bit input vector, W = w3w2w1w0, one bit-position to the right when the control signal *Right* is equal to 1, and one bit-position to the left when the control signal *Left* is equal to 1. When *Right* = *Left* = 0, the output of the circuit should be the same as the input vector. Assume that the condition *Right* = *Left* = 1 will never occur.