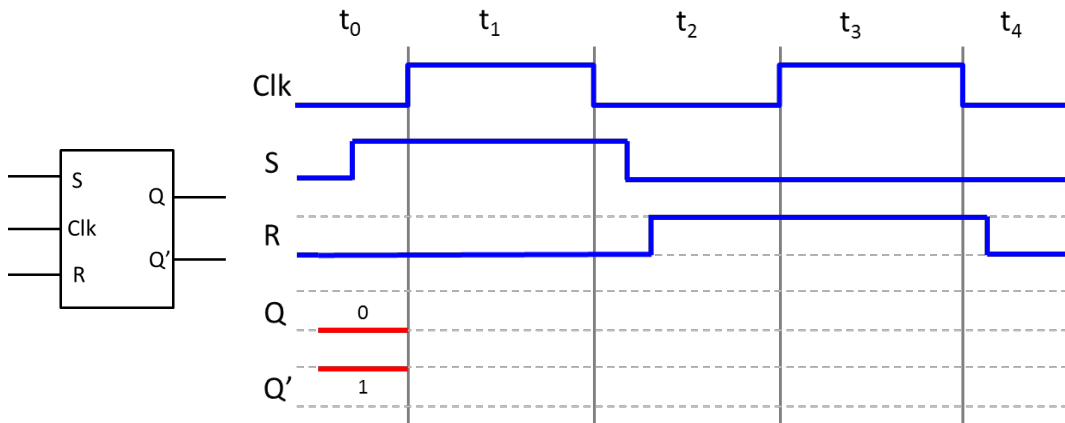
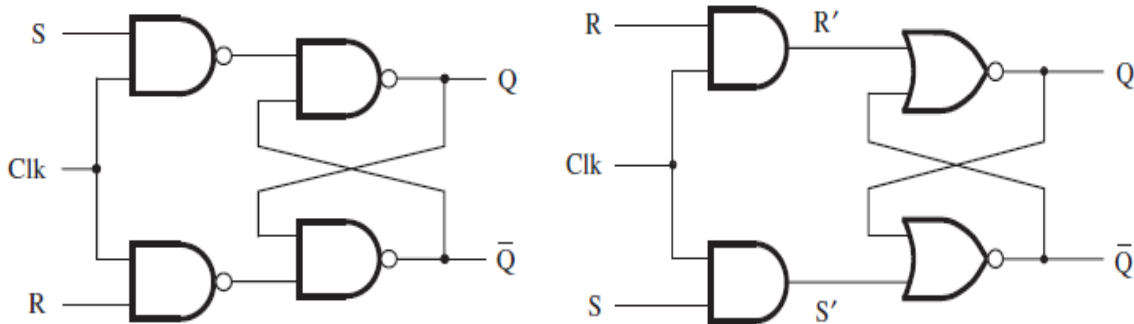


**P1. (5 points)** Complete the following timing diagram for a gated SR-latch. Assume that there's no gate delay.



- a) Describe what the circuit in P1 above does (i.e., how Q and P are changed) when:
- i.  $R=0, S=0$
  - ii.  $R=0, S=1$
  - iii.  $R=1, S=0$
  - iv.  $R=1, S=1$

**P2. (10 points)** Show that the gated SR latches in the two figures below are functionally equivalent by transforming the first figure to the second using the rules of Boolean algebra. Please show your transformation process step by step using circuit diagrams.



**P3. (20 points)** Consider the SR and the JK flip-flops

- a) An SR flip-flop has set and reset inputs like a gated SR latch. Show how an SR flip-flop can be constructed using a D flip-flop and other logic gates.
- b) Show how a JK flip-flop can be constructed using a T flip-flop and other logic gates.

**P4. (15 points)** Given a 100-MHz clock signal, derive a circuit using D flip-flops to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming reasonable delays.

**P5. (20 points)** Consider the following truth table for the function  $f(a,b,c,d)$ .

$a$	$b$	$c$	$d$	$f$
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

- (10 points) Implement  $f$  using one 4-to-16 decoder and a minimal number of gates.
- (10 points) Implement  $f$  using one 8-to-1 multiplexer and a minimal number of gates.

**P6. (10 points)** Implement the circuit for an 8-to-1 multiplexer using a 3-to-8 decoder and other necessary gates. The circuit should have control inputs  $s_2, s_1, s_0$ , data inputs  $w_7, w_6, w_5, w_4, w_3, w_2, w_1, w_0$ , and an output  $f$ .

**P7. (10 points)** A full adder has inputs  $X, Y, C_{in}$  and outputs  $S$  and  $C_{out}$ .

- Write the truth table for the full adder.
- Implement the circuit for the output  $S$  by using one 4-to-1 multiplexer and a minimal number of other logic gates.
- Implement the circuit for the output  $C_{out}$  by using one 4-to-1 multiplexer. Please use  $x$  and  $y$  as the select lines  $s_1$  and  $s_0$  of the multiplexer.

**P8. (10 points)** Use Shannon's Expansion to implement the following functions:

- $F(x,y,z,w) = \sum m(1,2,4,7,8,11,13,14)$  with only 4x1 Multiplexers.
- $F(x,y,z,w) = \sum m(0,3,5,6,9,10,12,15)$  with only 2x1 Multiplexers.