Cpr E 281 HW07
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Arithmetic Circuits and Combinational-Circuit Building Blocks
Assigned Date: Eighth Week
Due Date: Oct. 16, 2017

P1. (18 points) Using IEEE 754 SINGLE-PRECISION FLOATING-POINT FORMAT

(a) Represent the decimal number 13.5 in IEEE 754 single-precision floating-point format.
(b) Represent the decimal number 15.625 in IEEE 754 single-precision (32 bit) floating-point format.
(c) Represent the decimal number -0.75 in IEEE 754 single-precision (32 bit) floating-point format.
(d) What is the decimal value of the following IEEE 754 single-precision floating-point number? 1 0111111 00101000 00000000 00000000
(e) What is the decimal value of the following IEEE 754 single-precision floating-point number? 1 01111110 0110000 00000000 00000000
(f) What is the decimal value of the following IEEE 754 single-precision floating-point number? 1 10000001 01101000000000000000000

P2. (10 points) Prove that the following two circuits are different representations of the full-adder circuit.
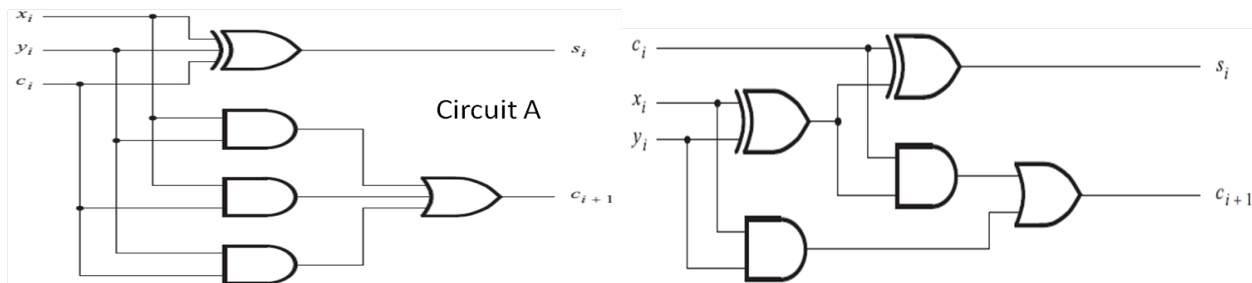
P3. (10 points) Consider constructing a 2n-to-1 multiplexer using only 2-to-1 multiplexers, with n being a positive integer.

(a) How many 2-to-1 multiplexers would a 2n-to-1 multiplexer require? Give an answer in terms of n.
(b) Design an 8-to-1 multiplexer ($8=2^3$) using a minimal number of 2-to-1 multiplexers. Please label all signals clearly.

P4. (10 points) This question considers the design of an 8-to-1 multiplexer using logic gates. Assume the data inputs are I0,...,I7 and the select inputs are S2, S1 and S0.

(a) Write a sum-of-products expression for the 8-to-1 multiplexer.
(b) Implement the expression in part (a) using NOT and NAND gates with any number of inputs. Please use as few gates as possible.

Cpr E 281 HW07
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Arithmetic Circuits and Combinational-Circuit Building Blocks
Assigned Date: Eighth Week
Due Date: Oct. 16, 2017

P5. (20 points) The following two examples illustrate how to implement NOT and AND functions with 2-to-1 multiplexers.
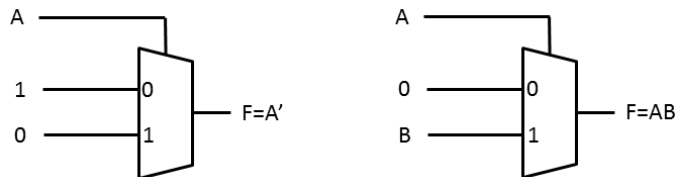
Use only 2-to-1 multiplexer to implement each of the following functions:

(a) (5 points) $F(A, B) = A + B$ (OR)

(b) (5 points) $F(A, B) = A \oplus B$ (XOR)

(c) (5 points) $F(A, B) = \overline{A \cdot B}$ (NAND)

(d) (5 points) $F(A, B) = \overline{A + B}$ (NOR)

Assume the inverse of each input variable is available. (i.e., you can directly use the inverse of each input variable A or B in your answer.)

P6. (15 points) Consider the function F that has 4 inputs A_3, A_2, A_1, A_0 such that the output of F is 1 if the unsigned binary number represented by $A_3 A_2 A_1 A_0$ is an integer divisible by 3 or 7 (i.e., 0, 3, 6, 7, 9, 12, 14 or 15). Otherwise, the output of F is 0.

(a) Write the truth table for F.

(b) Implement F using a 16-to-1 multiplexer and nothing else.

(c) Implement F using an 8-to-1 multiplexer, some AND gates, some OR gates, and some NOT gates.

P7. (7 points) Write the truth table for a 1-to-2 decoder (3 points). Draw a circuit that implements a 1-to-2 decoder using AND gates, OR gates and NOT gates only (4 points).

P8. (10 points) Given a supply of 2-to-4 decoders, show how to get a 4-to-16 decoder circuit. Assume each of the 2-to-4 decoders has an ENABLE input (ENABLE = 1 enables the decoder), but you need not include an enable capability on the 4-to-16 decoder circuit.