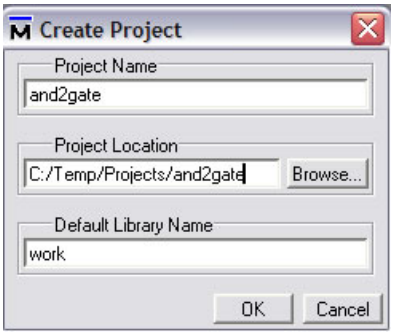
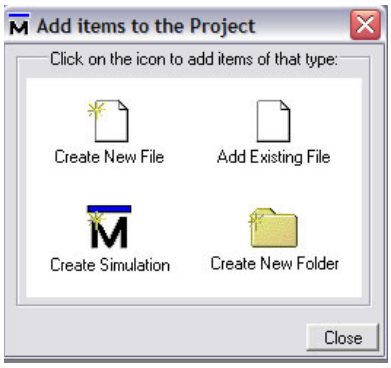
ModelSim SE 6.1b Tutorial

1. Start ModelSim
2. Create a new project
   - Click on *File*, then *New*, then choose *Project* on the drop down menu
   - Enter your project name, in this case the project is called “and2gate”
   - Choose your project location, this project is stored at “C:\Temp\Projects\and2gate”
   - The default library name should be *work*.
   - Click *OK* button

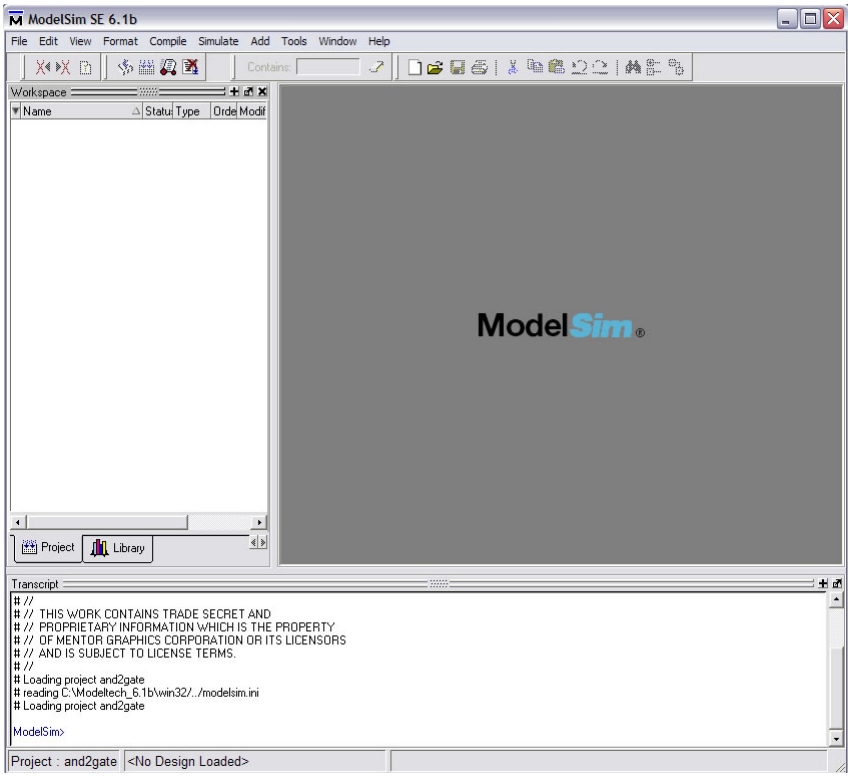


3. You will be asked if want to create the project directory.
   - Click *OK* button

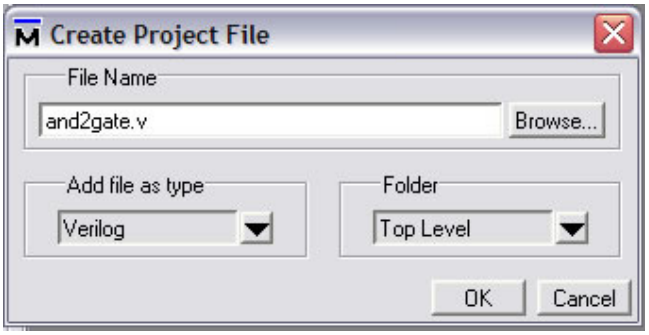
4. Next you will be presented with the Add Items to Project Dialog. While you can use this dialog to create new source files of add existing ones, we will not be using this option for the tutorial. We’ll add source files later so just click on the *Close* button



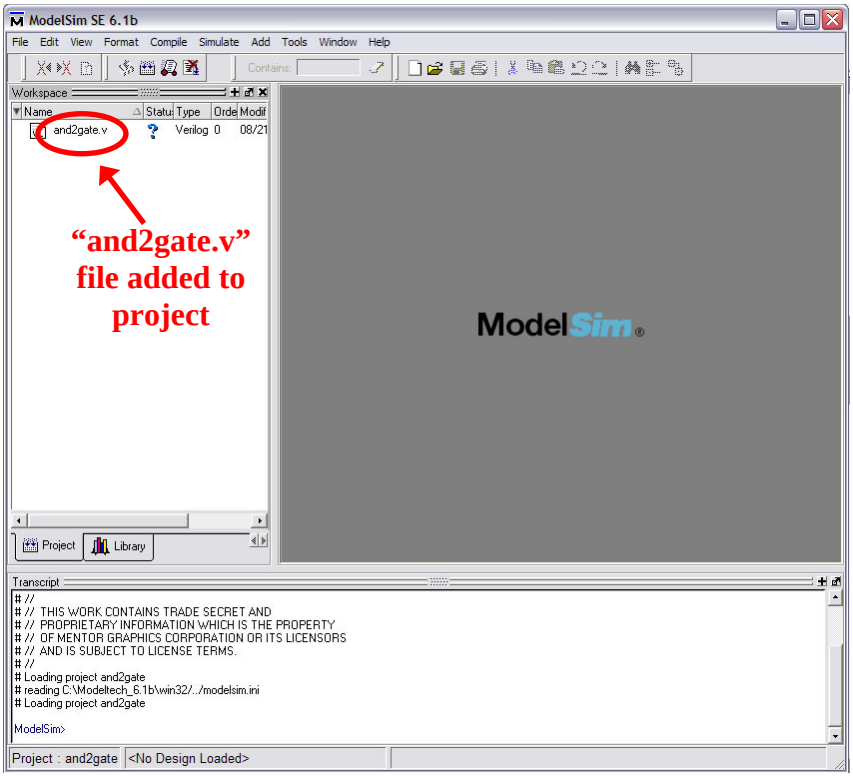
5. You now have a project by the name of “and2gate”.



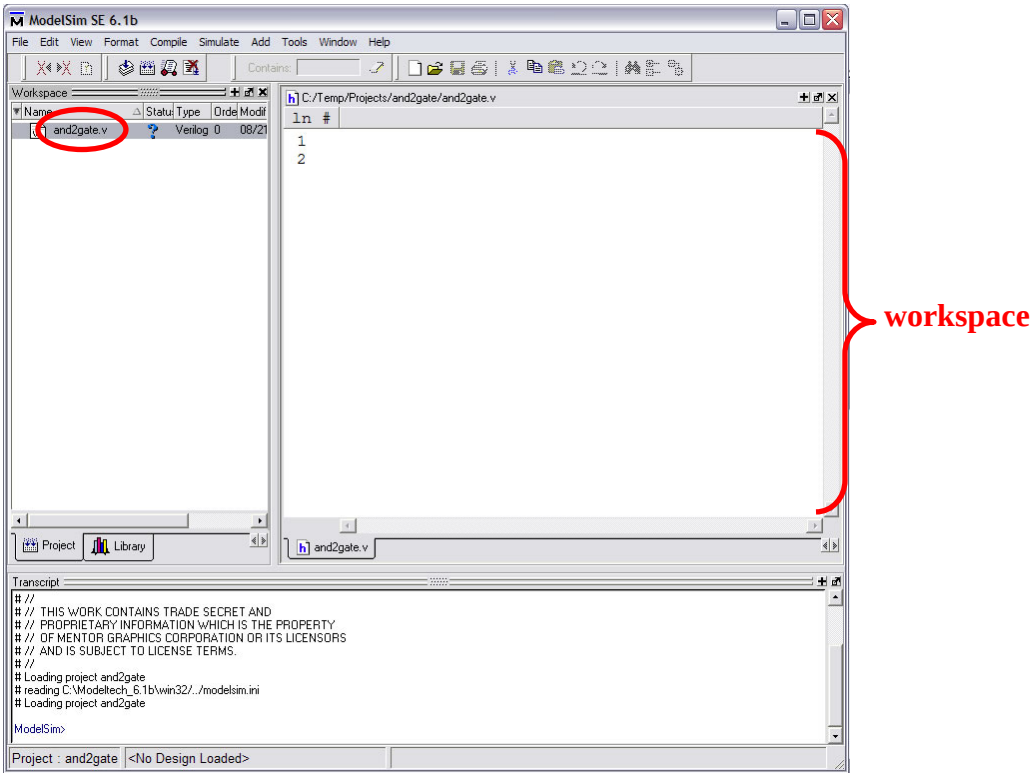
6. Now we want to add a new file to our project.
   - Click on *File*, choose *Add to Project*, and choose *New File…*
   - Choose *Verilog* as the file type
   - In the *File name:* box enter the desired file name, in this case the file is named “and2gate.v”
   - Click on the *OK* button



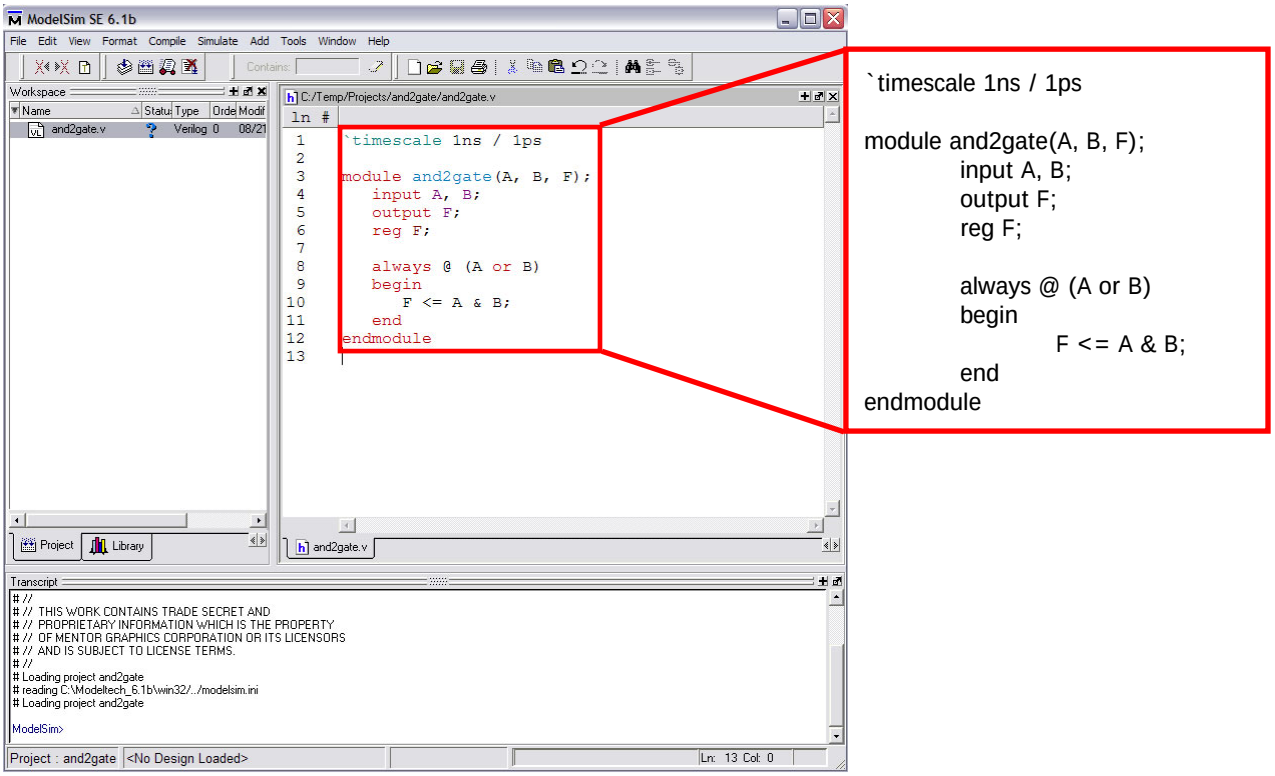
7. The “and2gate.v” file has been added to your project.



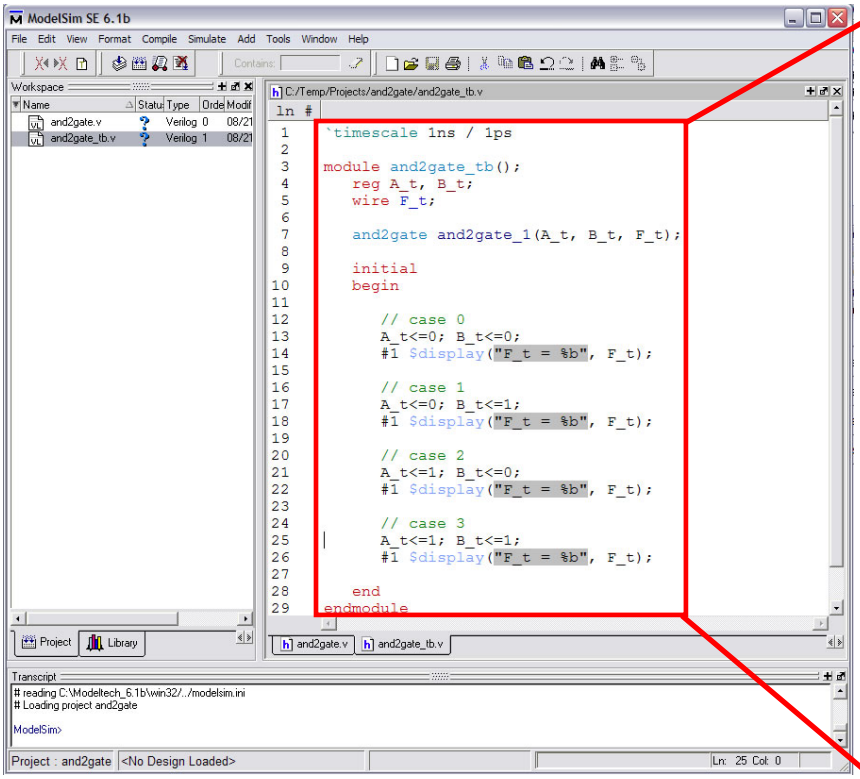
8. Double-click on the and2gate.v to show the file contents. You are now ready to specify the and2gate module’s functionality.



9. We compete the and2gate specification as shown below..
   - The line "`timescale 1ns/ 1ps" is located at the top of the file. The Verilog language uses dimensionless time units, and these time units are mapped to "real" time units within the simulator. `timescale is used to map to the "real" time values using the statement `timescale <time1> / <time2>, where <time1> indicates the time units associated with the #delay values, and the <time2> indicates the minimum step time used by the simulator. ***Note:*** Be sure to use the correct ` character. The ` is the not the single quotation mark (') and is typically located on the same key as the ~. If you have errors in your file, this may be the culprit.
   - The and2gate module is also declared using "module and2gate();" and "endmodule", but the ports are left for us to define.
   - Be sure to save the changes to the and2gate.v file by clicking on *File* and choosing *Save*.

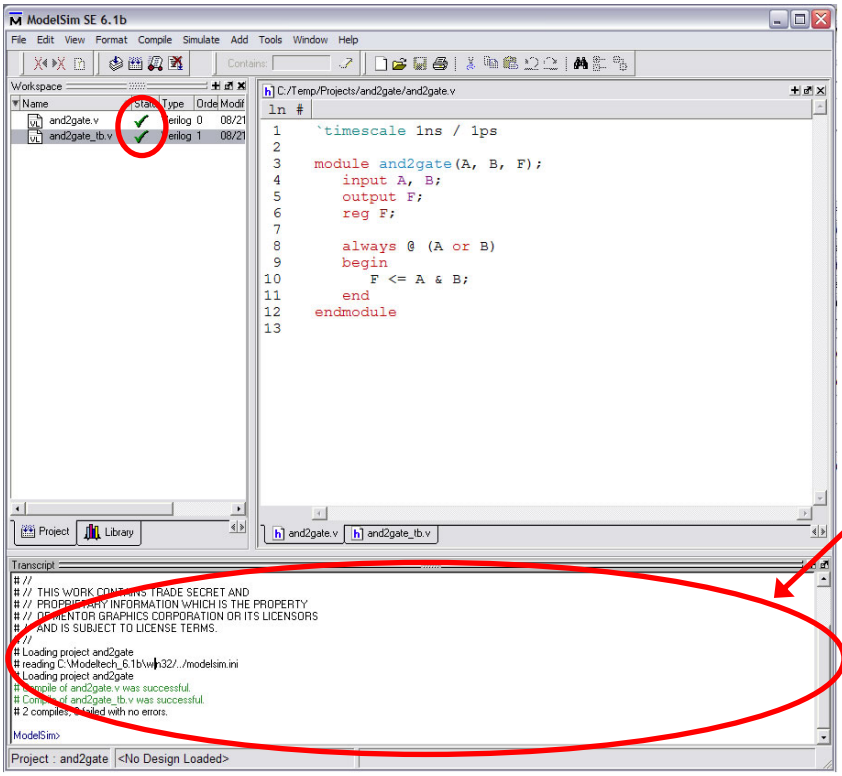


10. We also want to add a testbench and again follow Steps 6 – 9 to add “and2gate_tb.v”. Then we add the functionality of the testbench module as shown below.



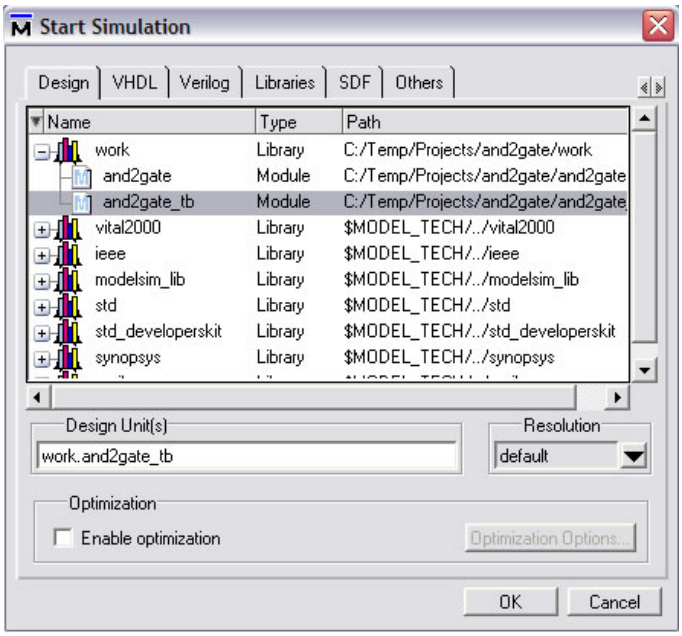

```
`timescale 1ns / 1ps

module and2gate_tb();
  reg A_t, B_t;
  wire F_t;

  and2gate and2gate_1(A_t, B_t, F_t);

  initial
  begin

    // case 0
    A_t<=0; B_t<=0;
    #1 $display("F_t = %b", F_t);

    // case 1
    A_t<=0; B_t<=1;
    #1 $display("F_t = %b", F_t);

    // case 2
    A_t<=1; B_t<=0;
    #1 $display("F_t = %b", F_t);

    // case 3
    A_t<=1; B_t<=1;
    #1 $display("F_t = %b", F_t);

  end
endmodule
```

11. After saving both “and2gate.v” and “and2gate_tb.v”, we want to check the syntax of both files.
    - Click on the *Compile* Menu and select *Compile All*
    - If the syntax was correct, a checkmark will appear next to each file
    - If the syntax was incorrect, the window at the bottom will list the individual errors.

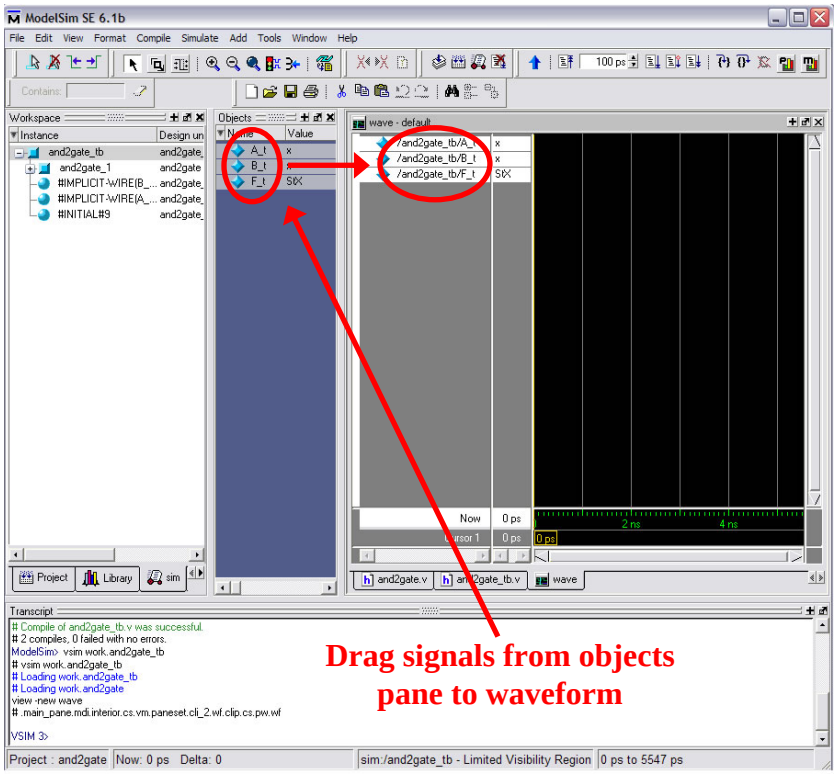


Any errors will be listed here

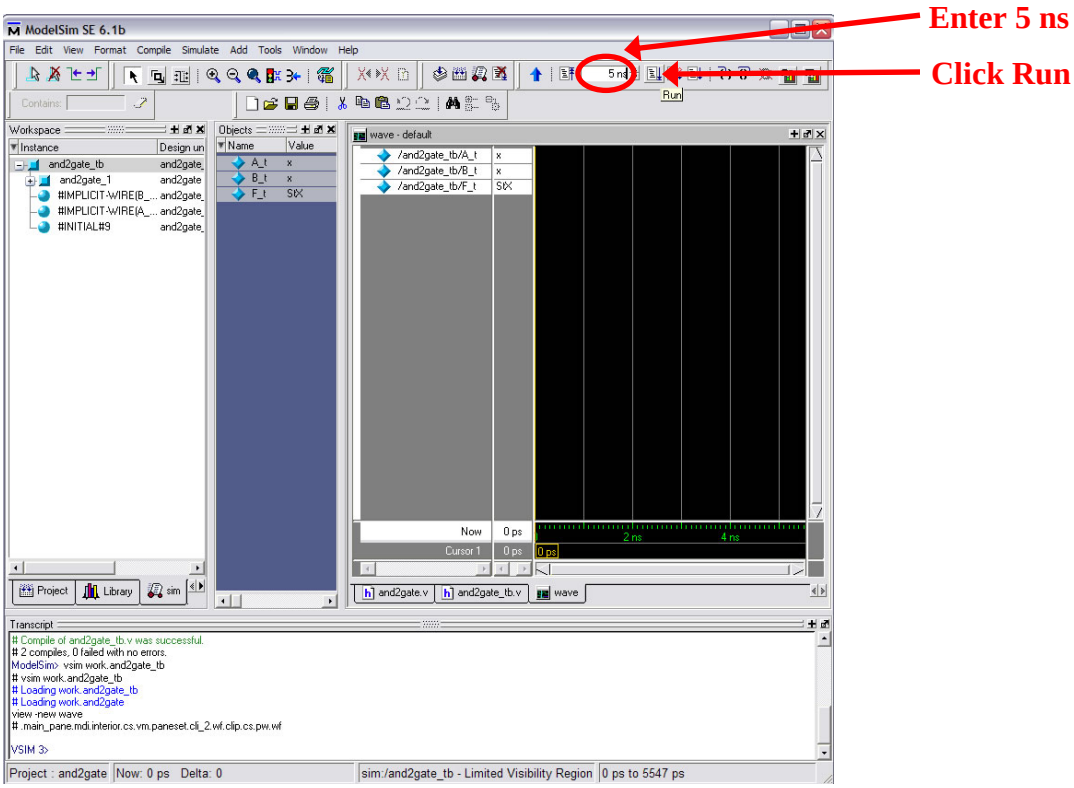
12. Now it’s time to simulate the design.
    - Click on the *Simulate* menu and choose *Start Simulation*
    - Expand the selection for the work library by click on the + symbol on the left.
    - Select and2gate_tb and click OK button



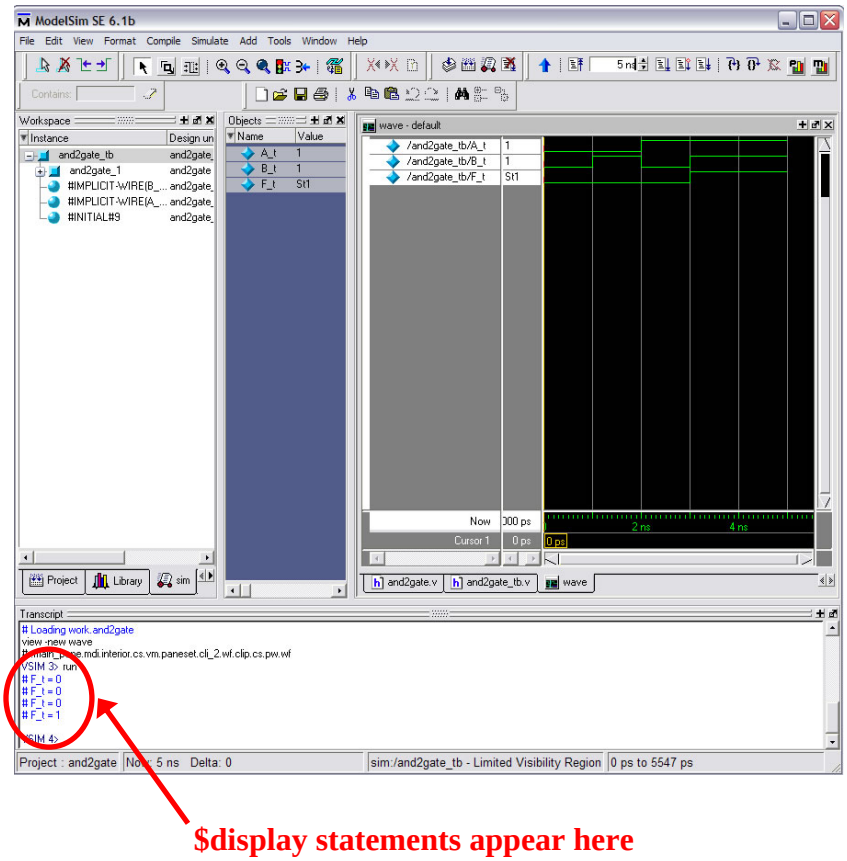
13. Next we create a simulation waveform window.
    - Click on *File* menu, choose *New*, then choose *Windows*, then choose *Wave*
    - Add the signals that would like to monitor by dragging the signal from the middle pane to the waveform window as shown below



14. We can simulate the design.
    - Enter 5 ns as the length of time we would like to simulate for in the Run Length box and click the Run icon as shown below.



15. Our simulation is complete. The simulation waveforms appear and we can check the and2gate module's functionality. Further, the $display statements included in the testbench appear in the lower window.



$display statements appear here