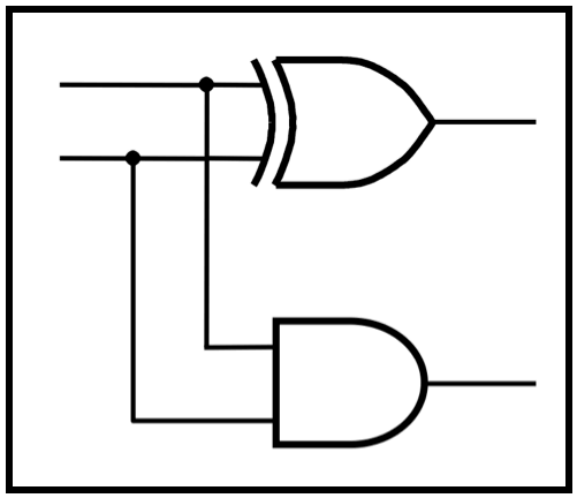

CprE 281: Digital Logic

Instructor: Alexander Stoytchev

http://www.ece.iastate.edu/~alexs/classes/

Mealy State Model

CprE 281: Digital Logic
Iowa State University, Ames, IA
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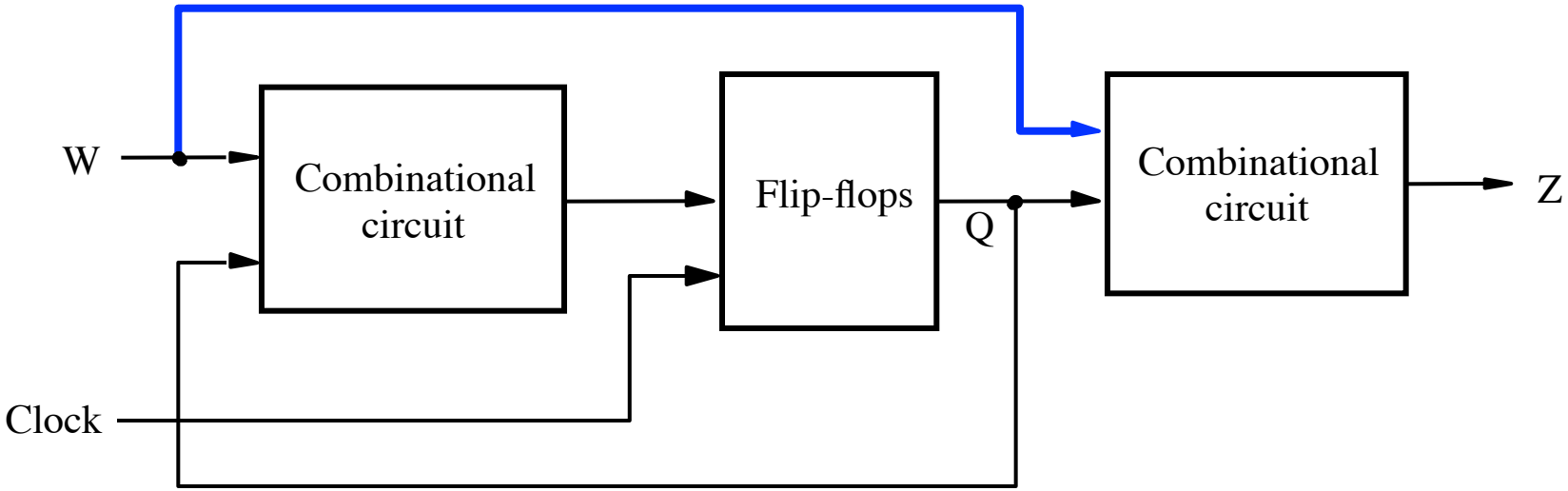
Administrative Stuff

- **Homework 10 is out**
- **It is due on Monday Nov 16 @ 4pm**

Administrative Stuff

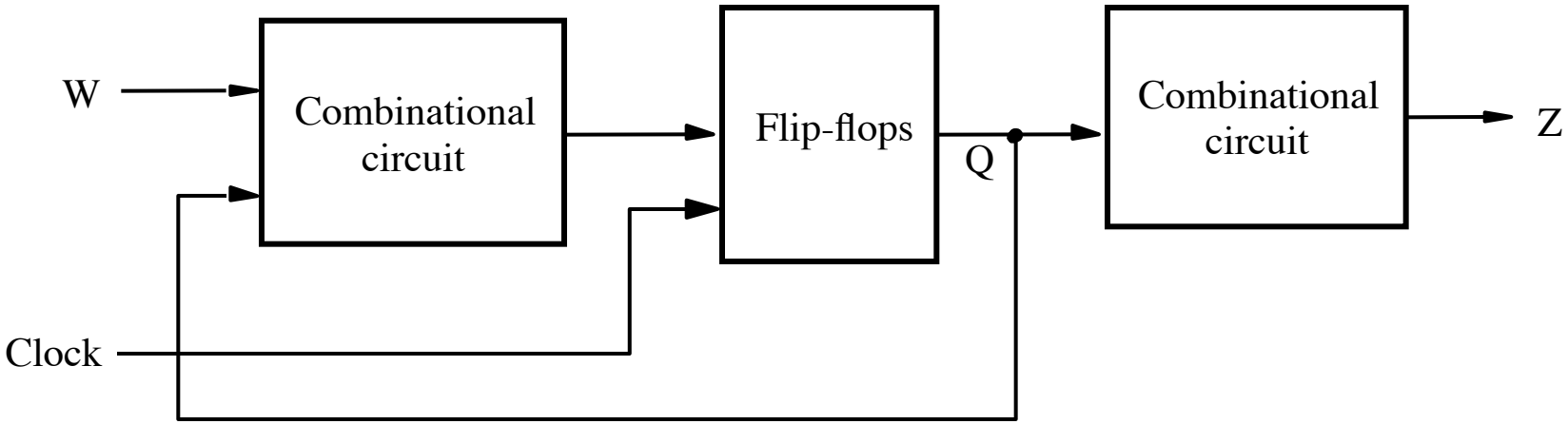
- **Final Project**

The general form of a synchronous sequential circuit

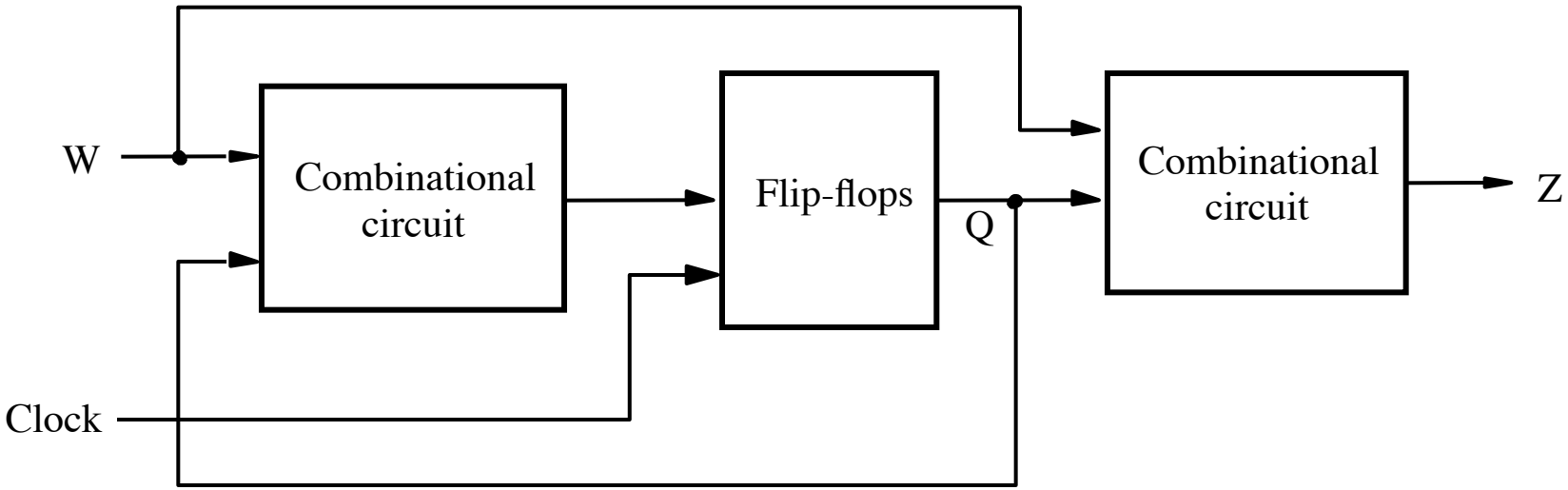


[Figure 6.1 from the textbook]

Moore Type


W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

Mealy Type


W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

Sample Problem

Implement a 11 detector. In other words, the output should be equal to 1 if two consecutive 1's have been detected on the input line. The output should become 1 as soon as the second 1 is detected in the input.

Sequences of input and output signals

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	1	0	0	1	1	0	0

[Figure 6.22 from the textbook]

Sequences of input and output signals

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

[Figure 6.22 from the textbook]

Sequences of input and output signals

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

[Figure 6.22 from the textbook]

Sequences of input and output signals

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

[Figure 6.22 from the textbook]

Sequences of input and output signals

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

[Figure 6.22 from the textbook]

Sequences of input and output signals

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

[Figure 6.22 from the textbook]

Sequences of input and output signals

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

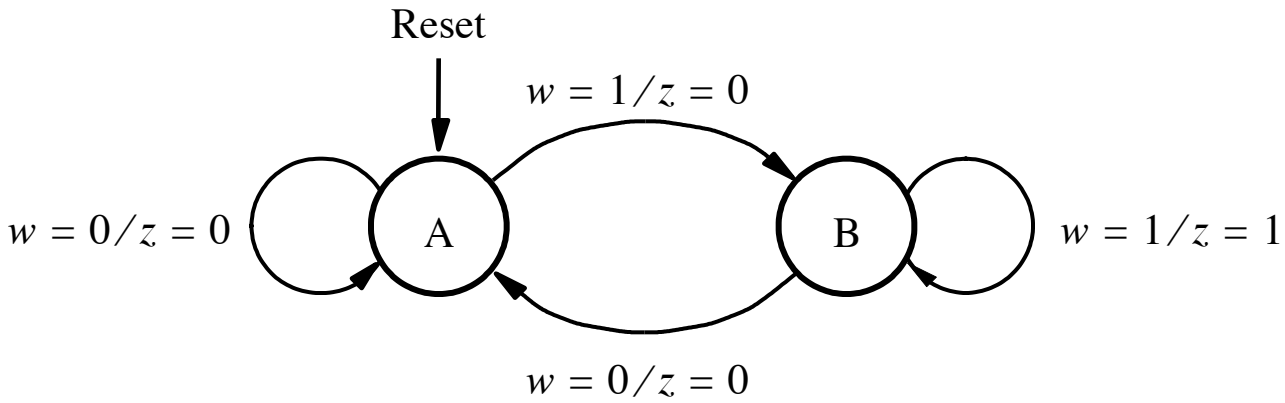
[Figure 6.22 from the textbook]

Sequences of input and output signals

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

[Figure 6.22 from the textbook]

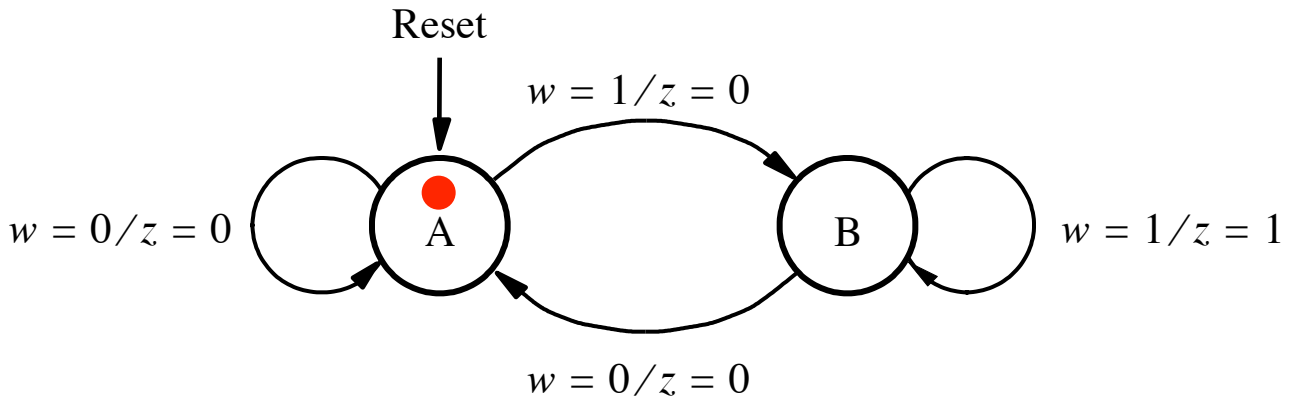
State diagram of an FSM that realizes the task



[Figure 6.23 from the textbook]

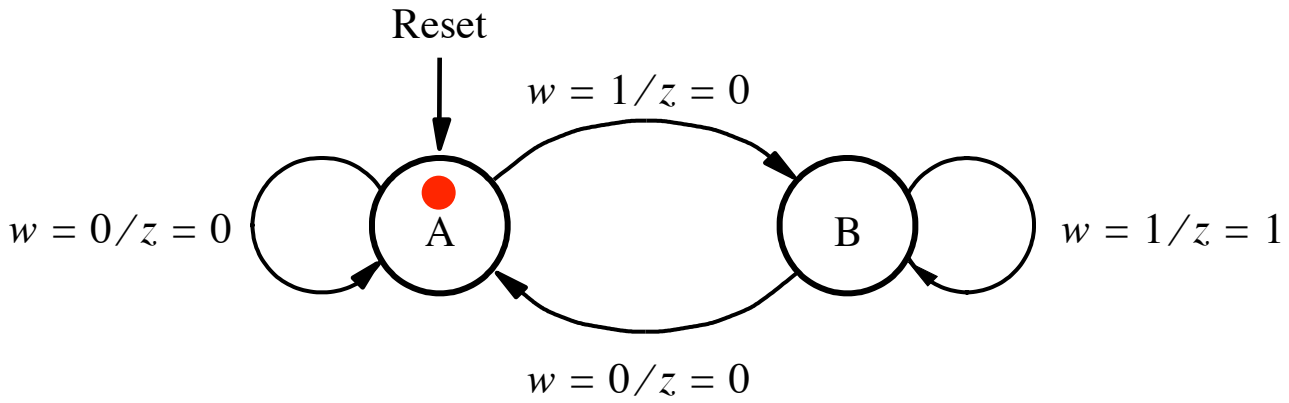
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



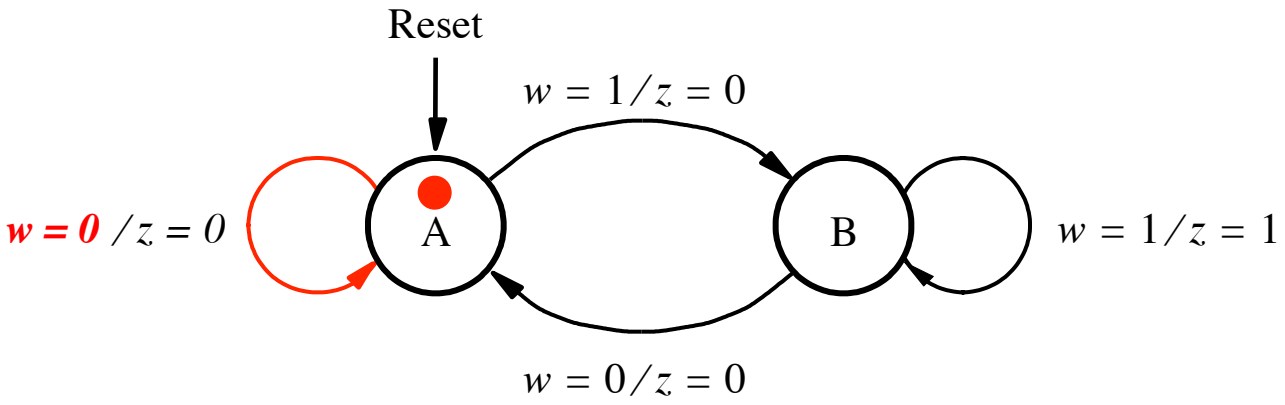
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



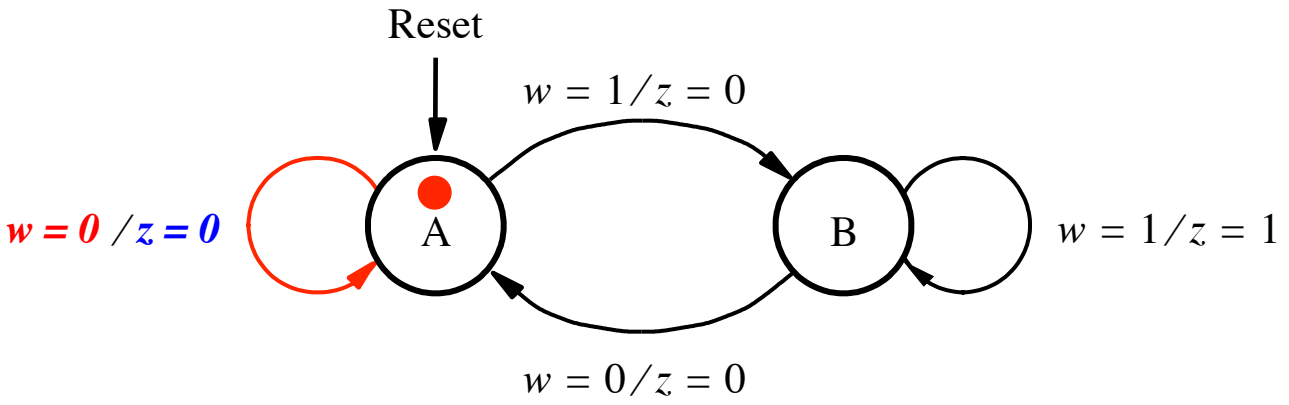
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



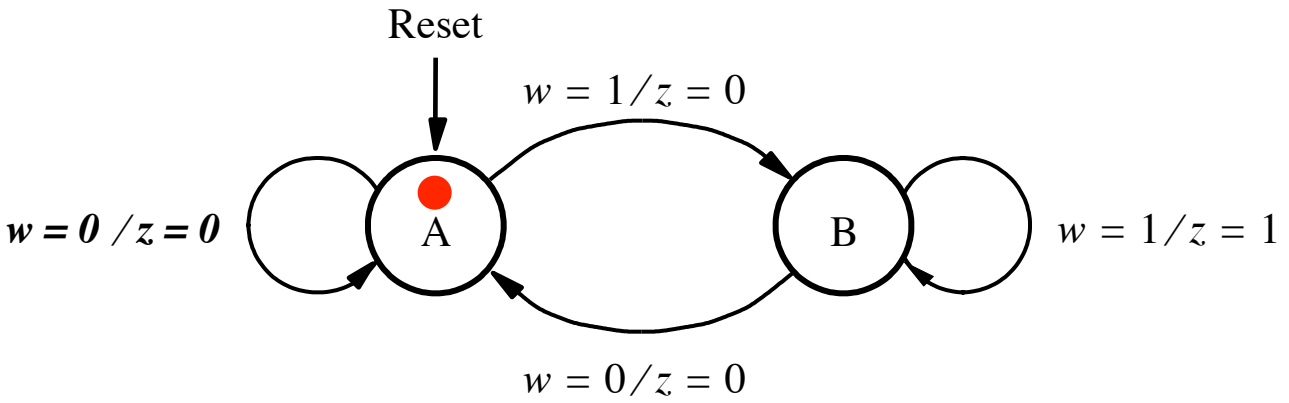
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



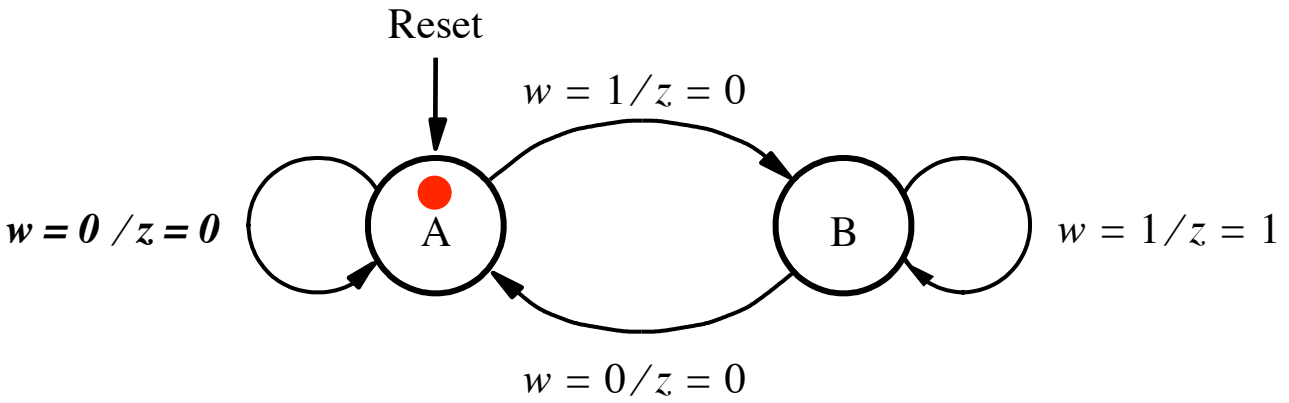
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



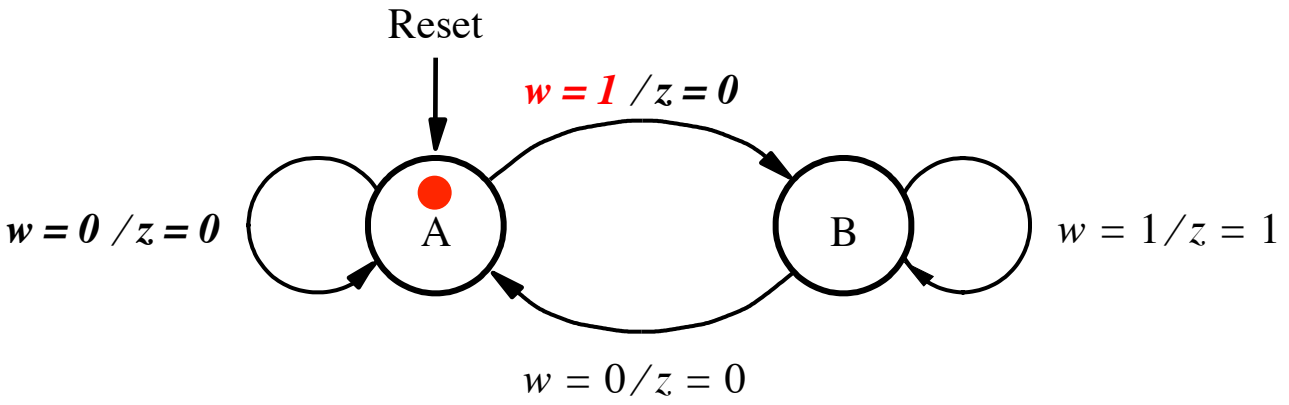
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



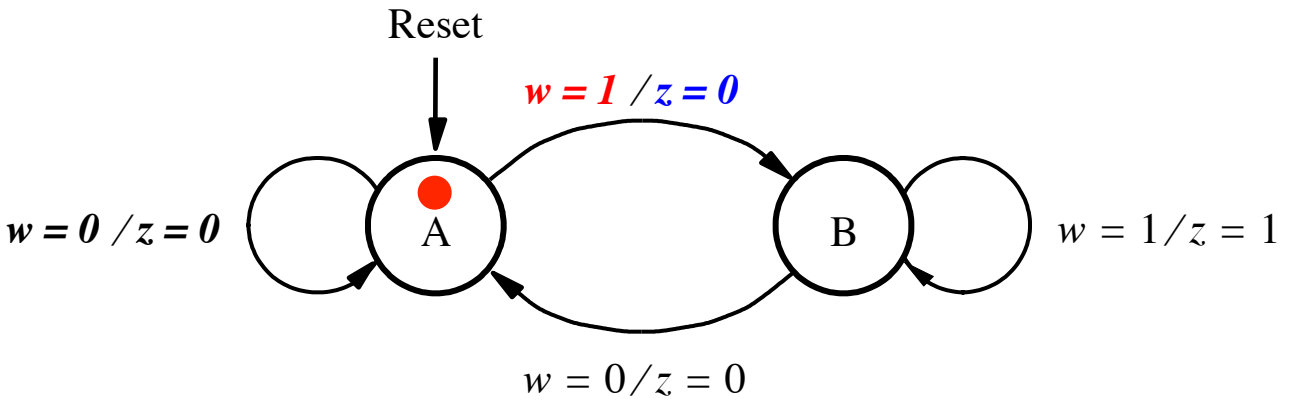
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



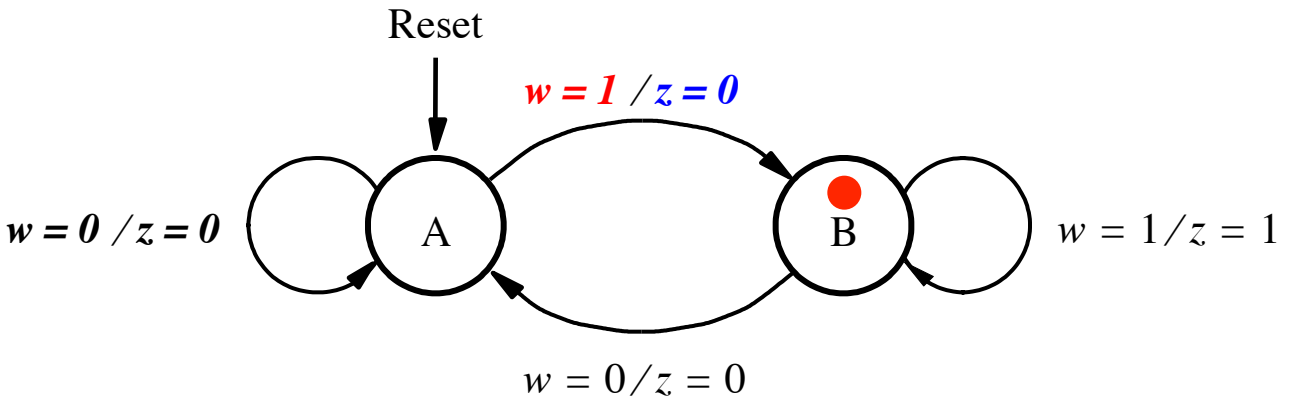
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



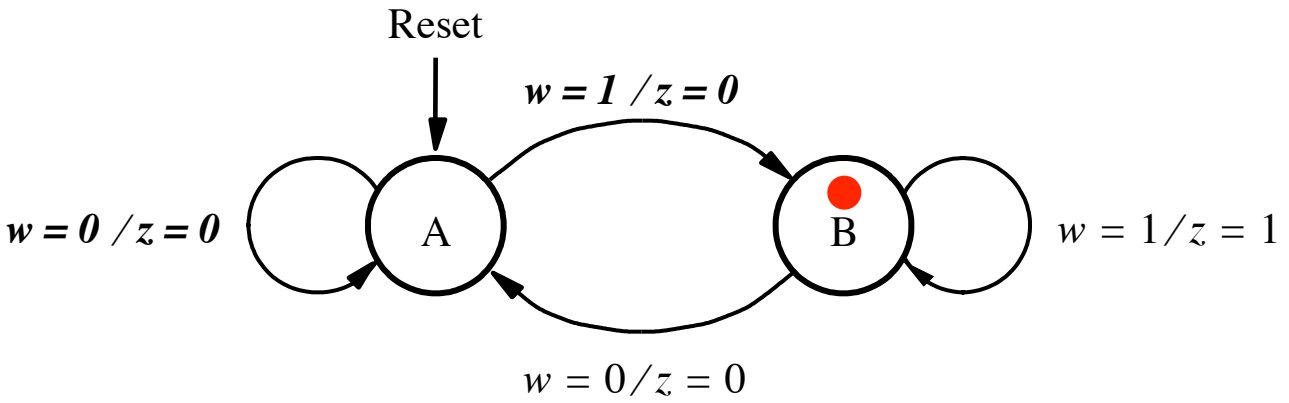
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



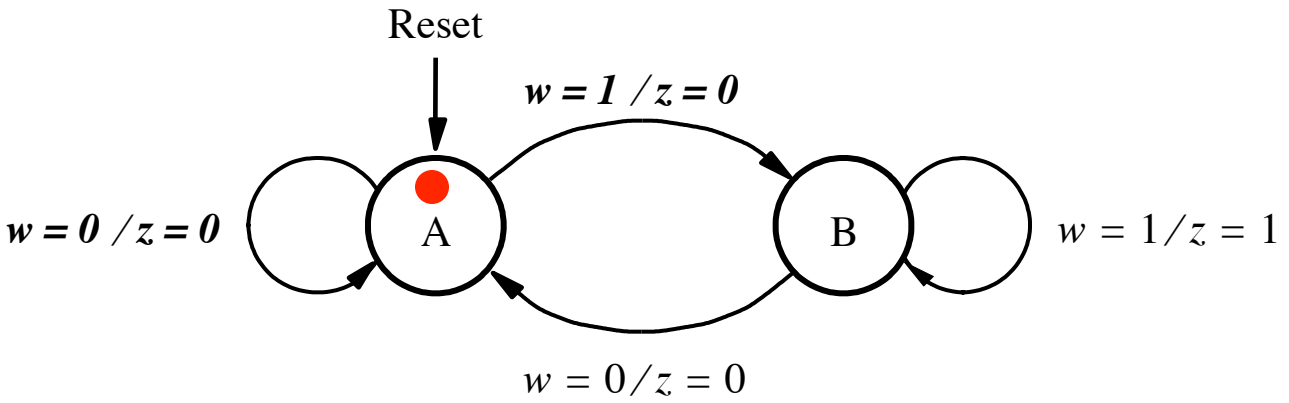
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



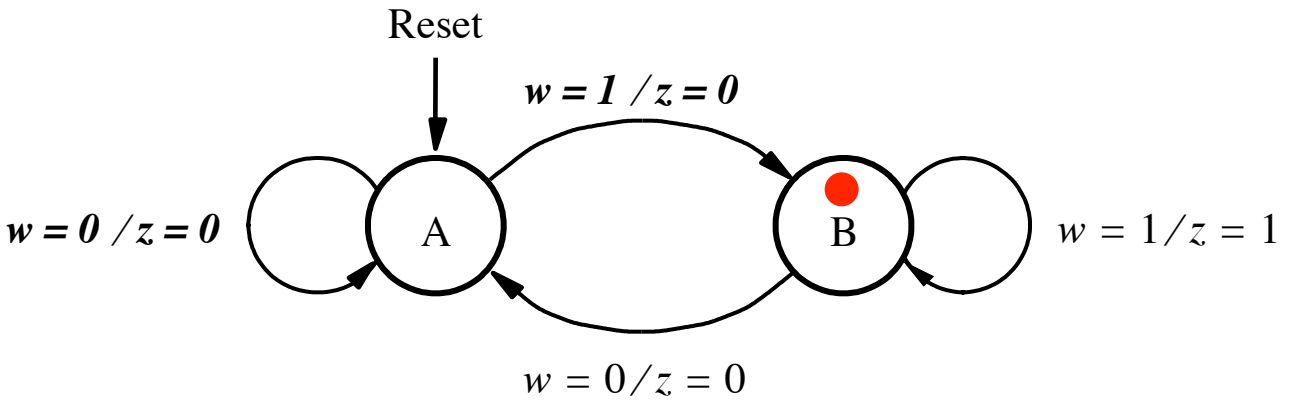
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



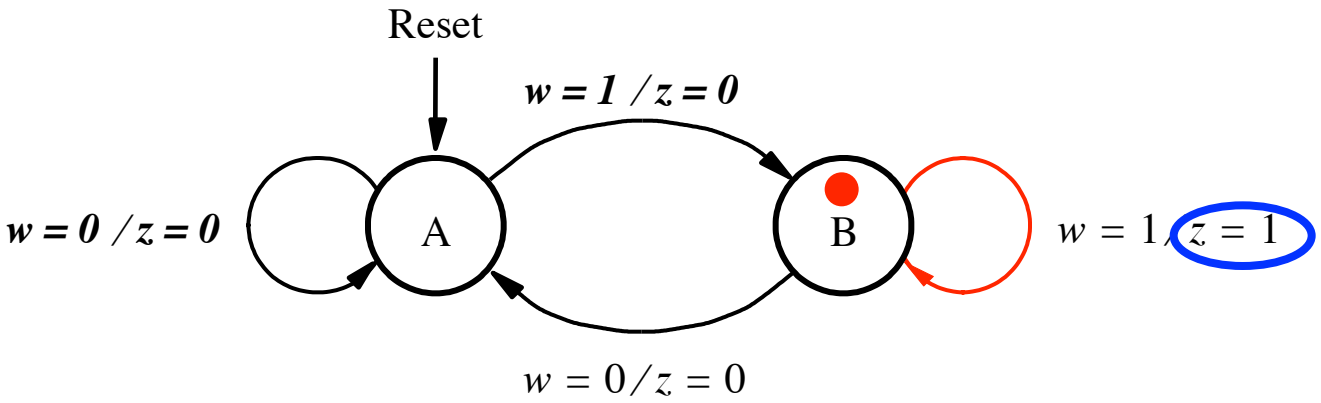
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



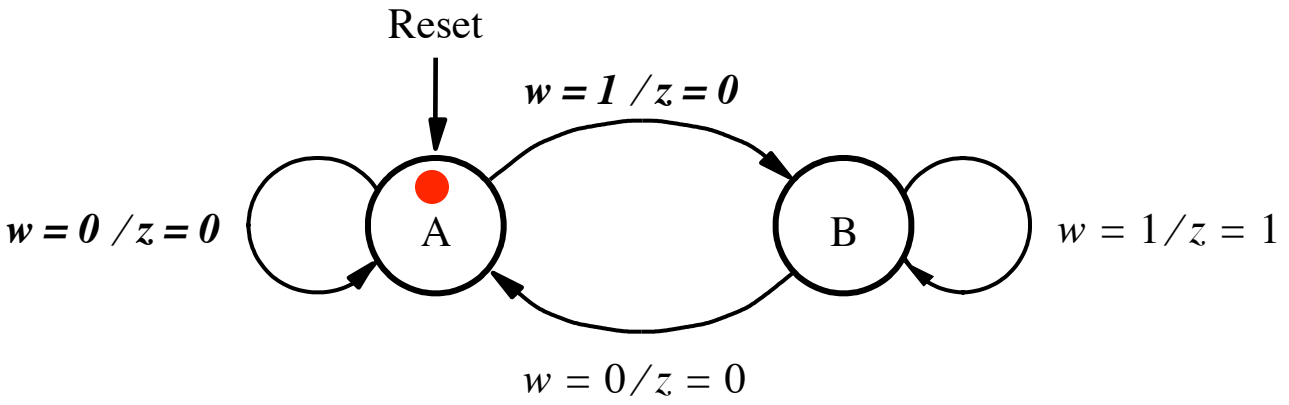
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



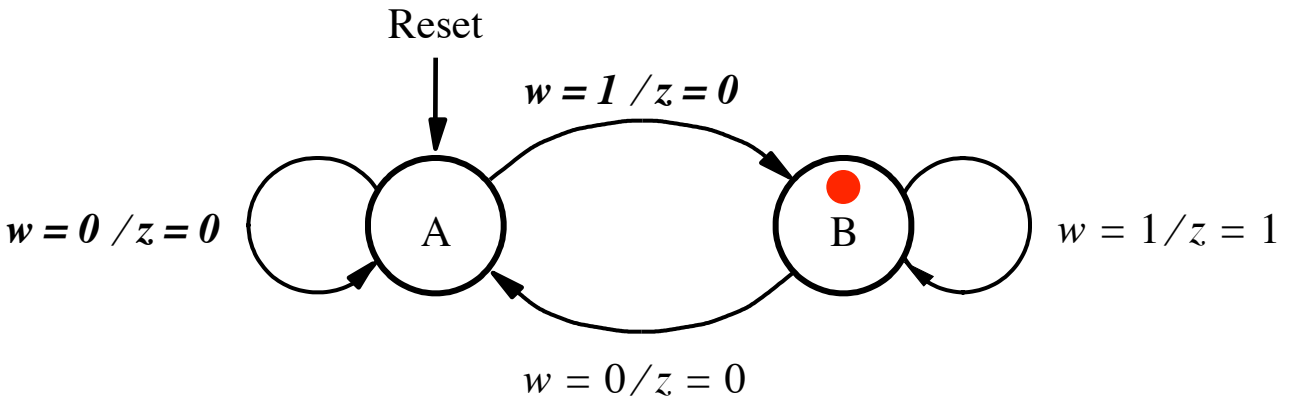
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



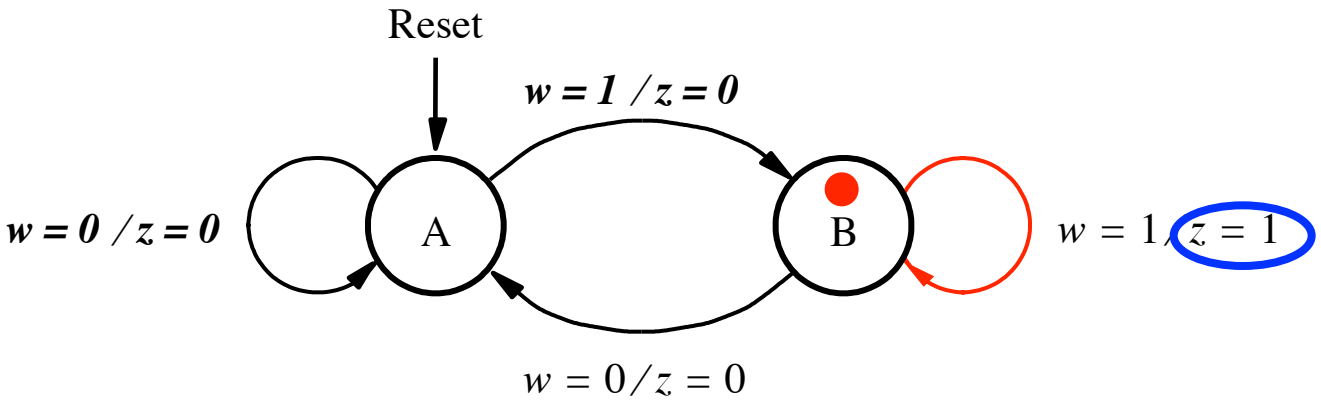
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



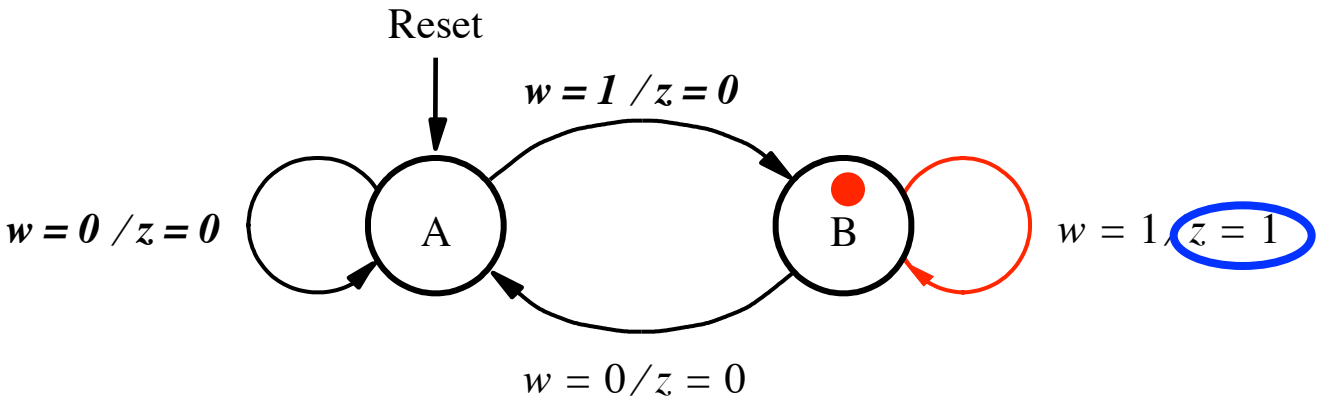
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



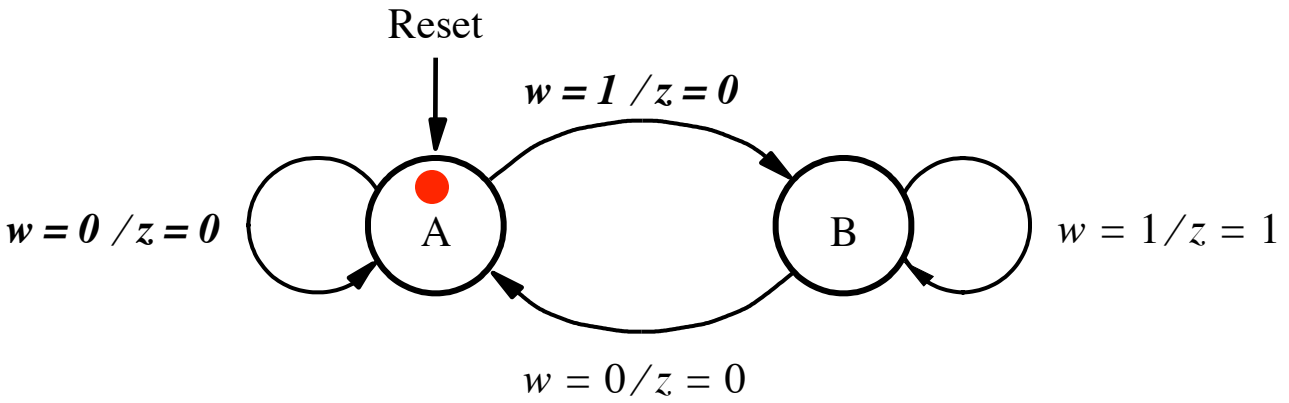
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



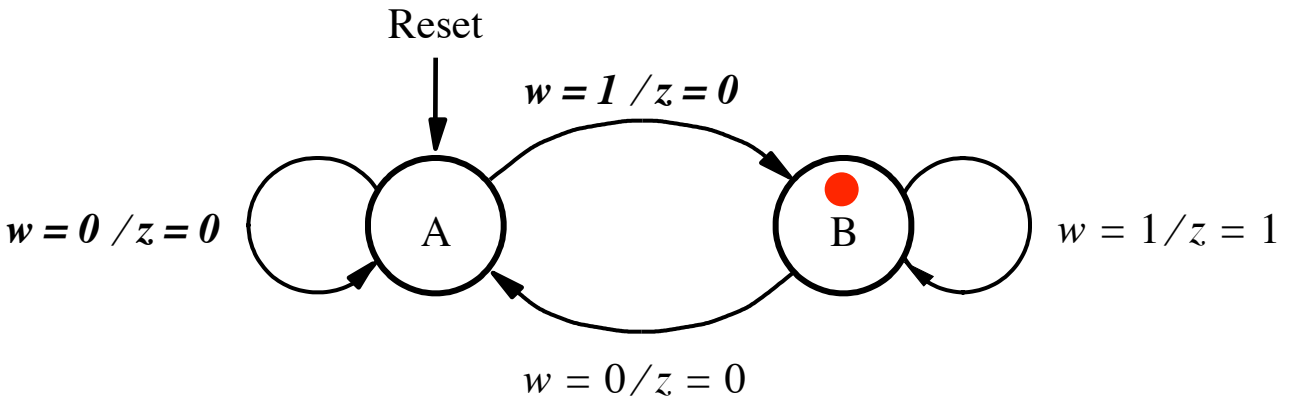
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

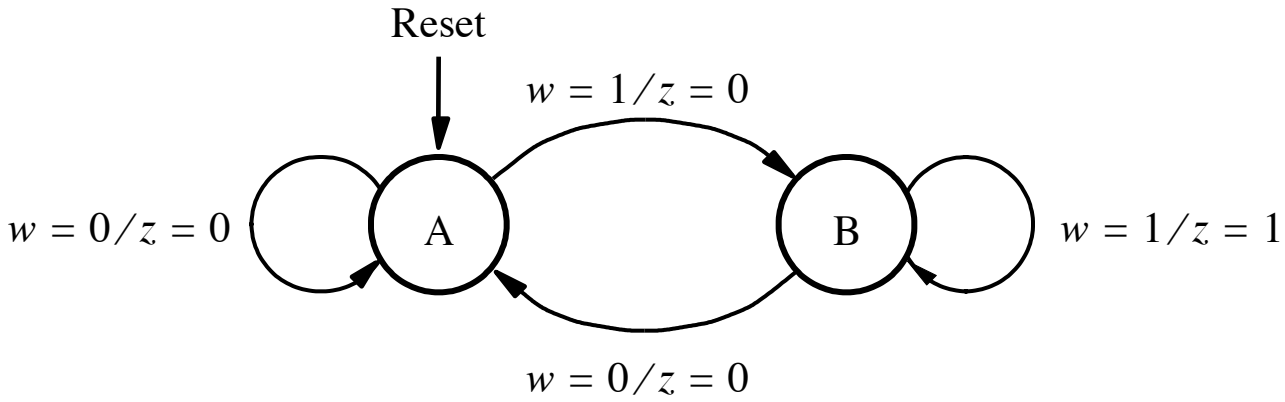


Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

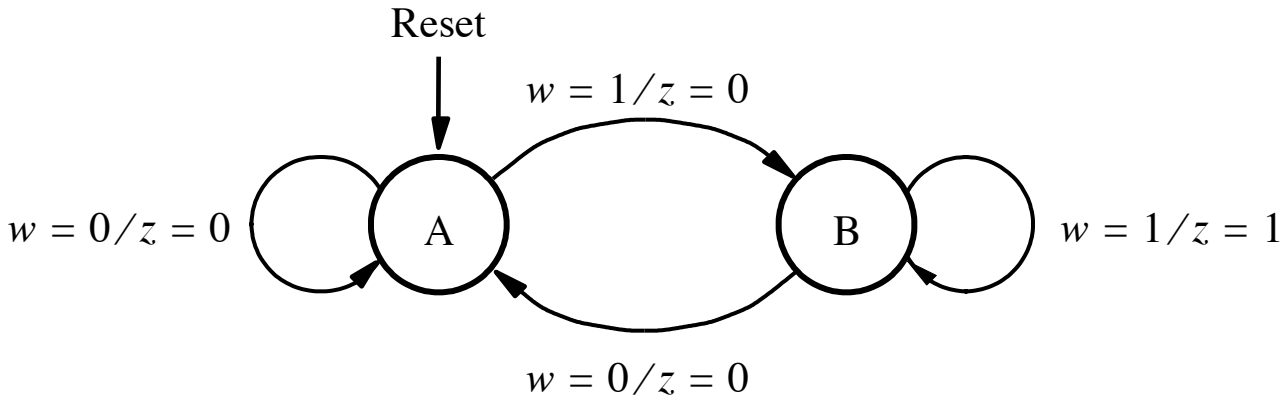


Now Let's Do the State Table for this FSM



Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A				
B				

Now Let's Do the State Table for this FSM



Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

The State Table for this FSM

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

[Figure 6.24 from the textbook]

Let's Do the State-assigned Table

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0				
B	1				

Let's Do the State-assigned Table

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

The State-assigned Table

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

[Figure 6.25 from the textbook]

The State-assigned Table

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

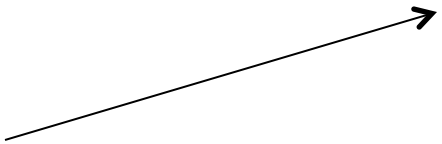
$$Y = D = w \qquad z = wy$$

[Figure 6.25 from the textbook]

The State-assigned Table

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

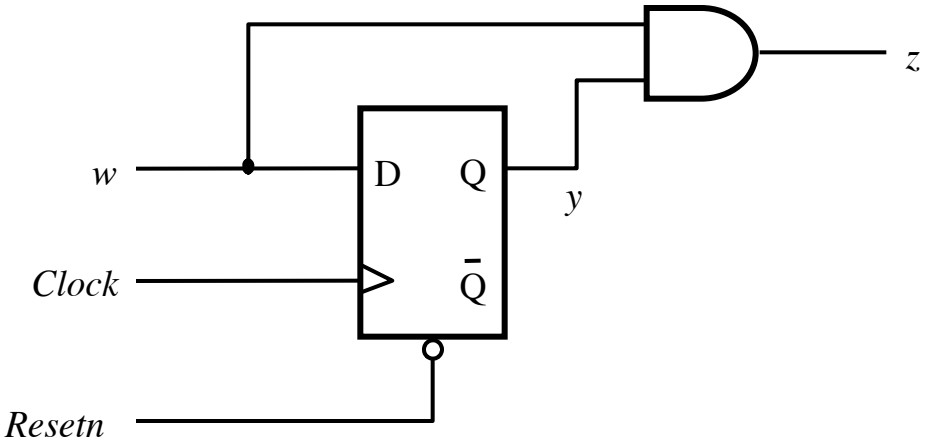
$Y = D = w$ $\quad\quad$ $z = wy$



This assumes D flip-flop

[Figure 6.25 from the textbook]

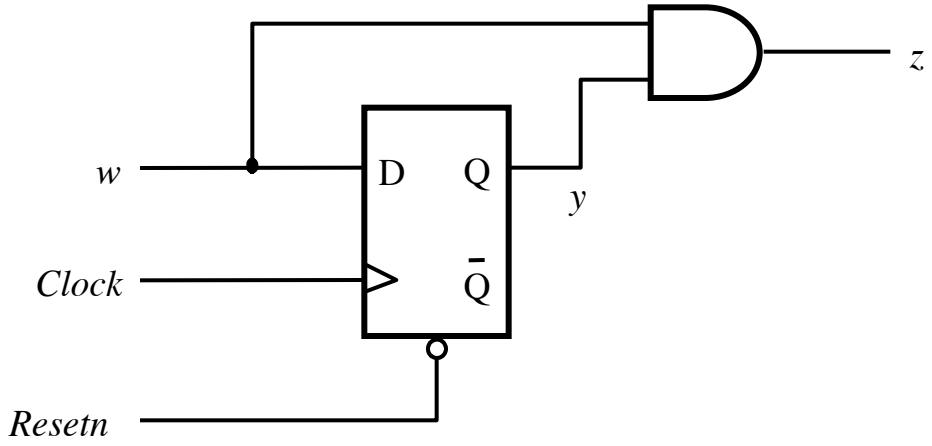
Circuit Implementation of the FSM



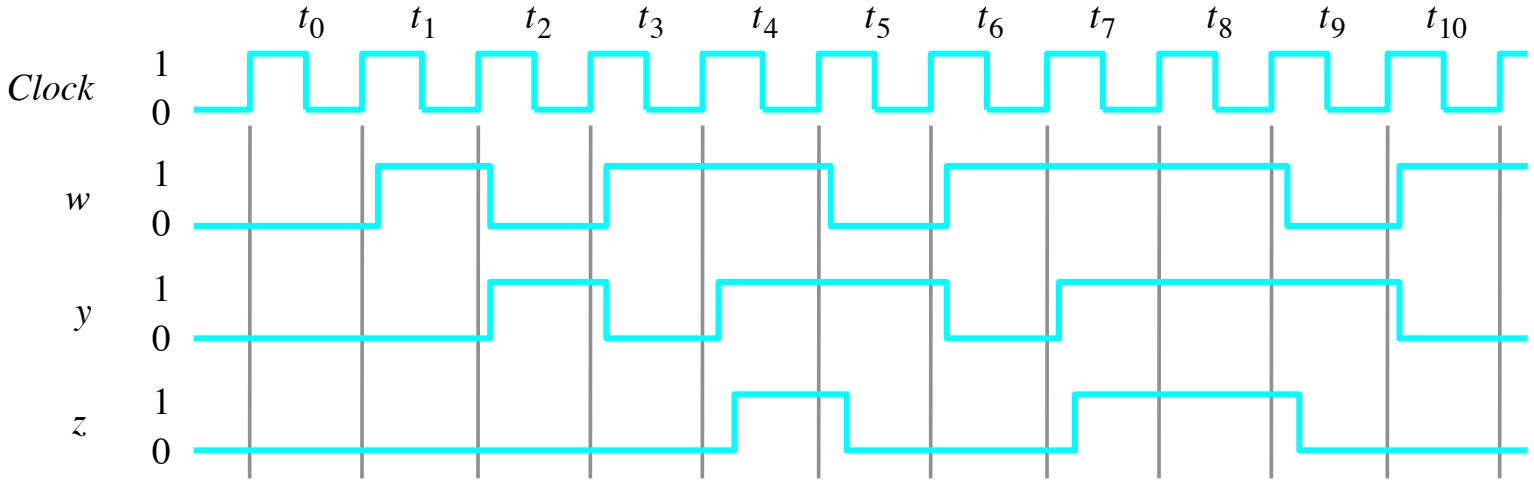
$$Y = D = w \qquad z = wy$$

[Figure 6.26 from the textbook]

Circuit & Timing Diagram



(a) Circuit

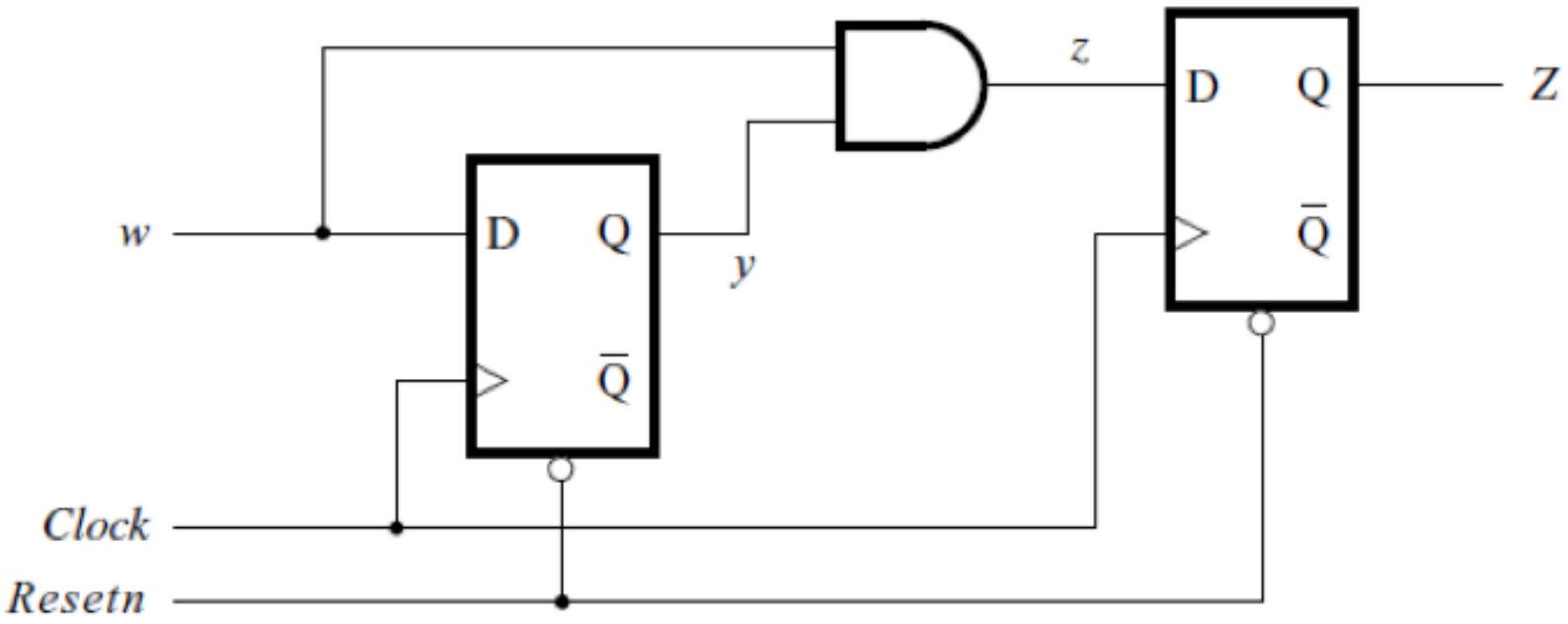


(b) Timing diagram

[Figure 6.26 from the textbook]

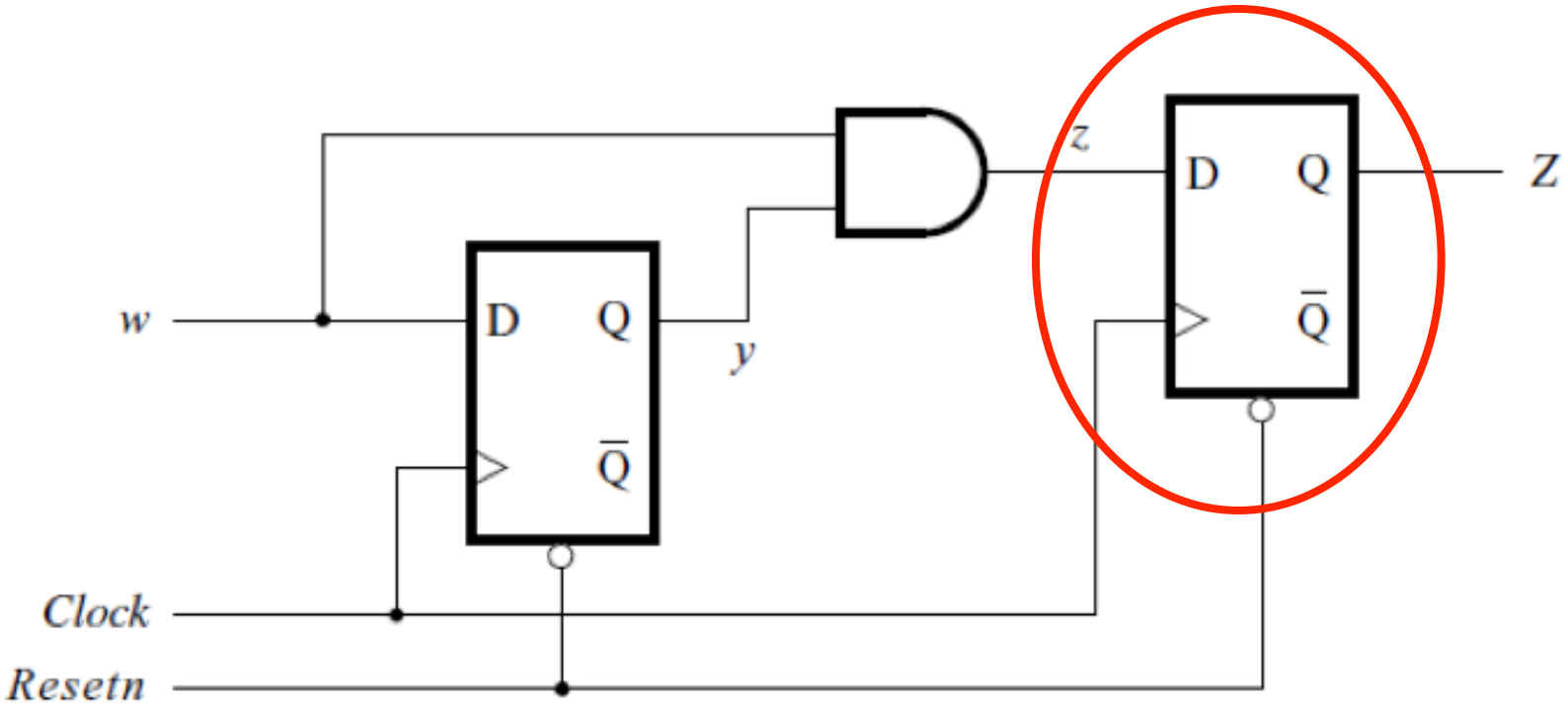
What if we wanted the output signal to be delayed by 1 clock cycle?

Circuit Implementation of the Modified FSM



[Figure 6.27a from the textbook]

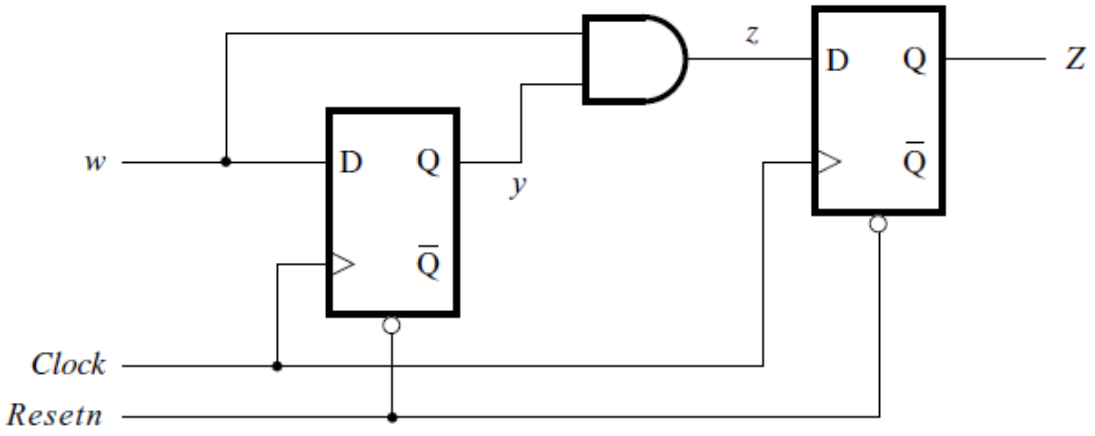
Circuit Implementation of the Modified FSM



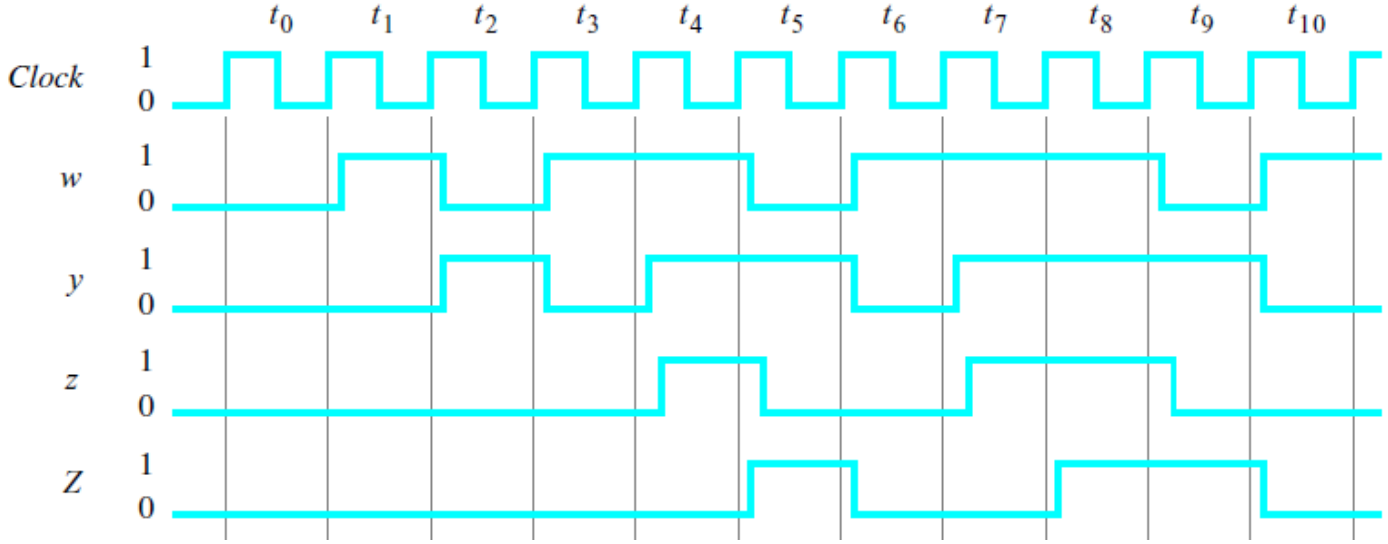
This flip-flop delays the
output signal by one clock cycle

[Figure 6.27a from the textbook]

Circuit & Timing Diagram

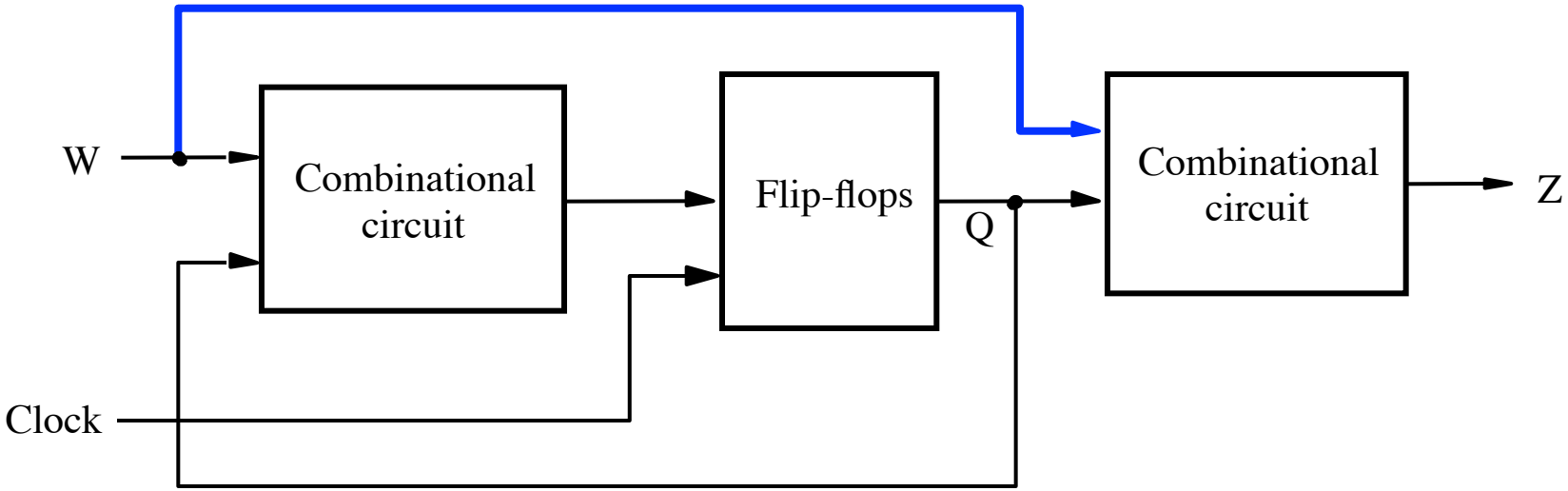


(a) Circuit



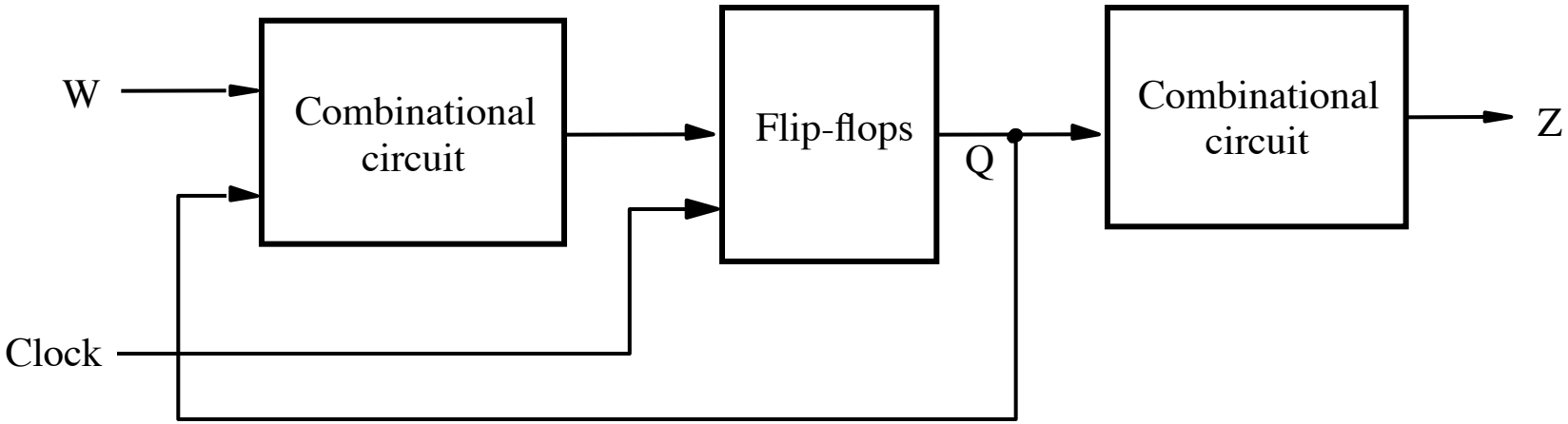
[Figure 6.27 from the textbook]

The general form of a synchronous sequential circuit

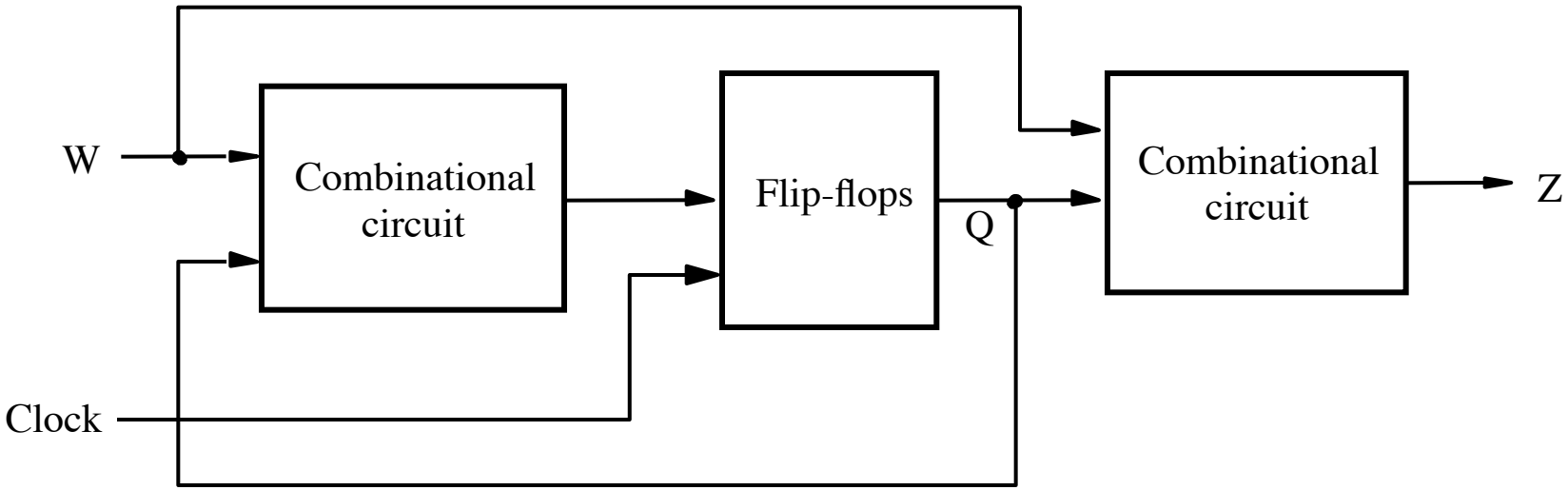


[Figure 6.1 from the textbook]

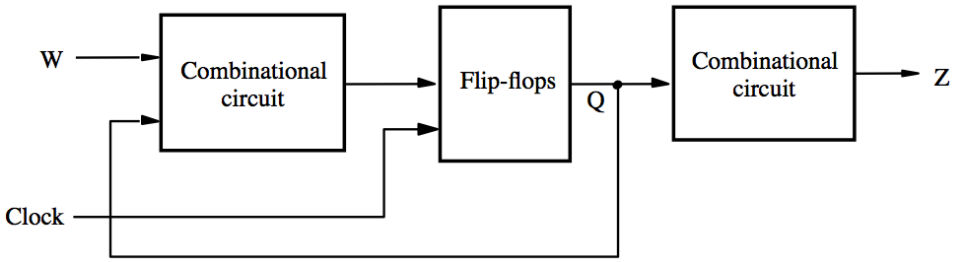
Moore Type


W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

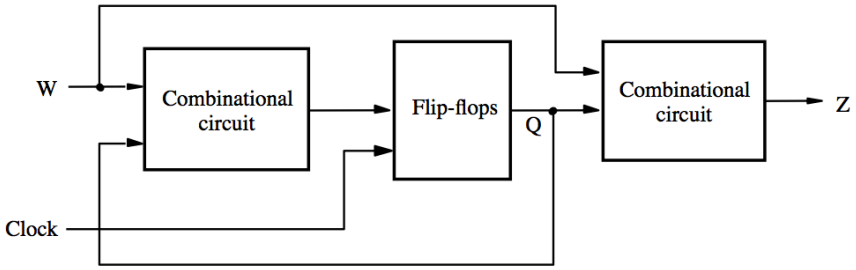
Mealy Type


W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

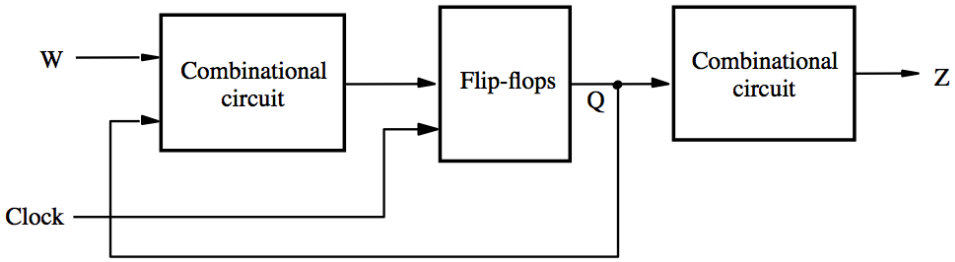
Moore

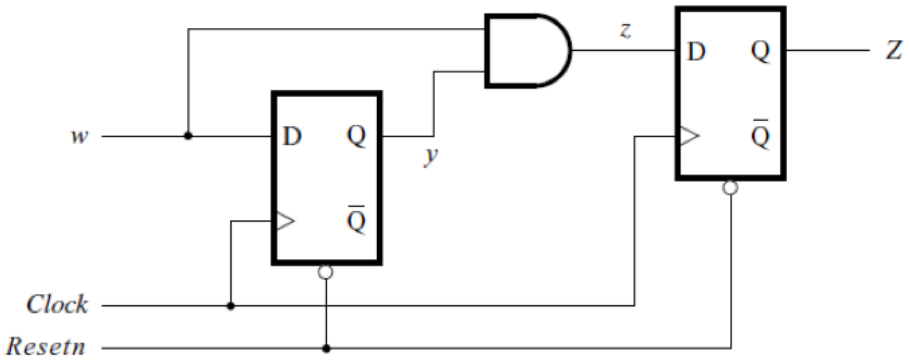

W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

Mealy

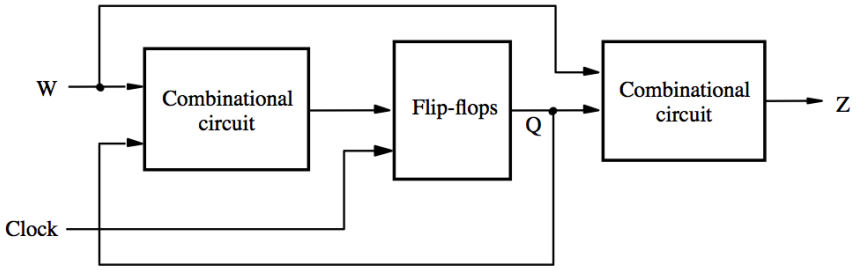

W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

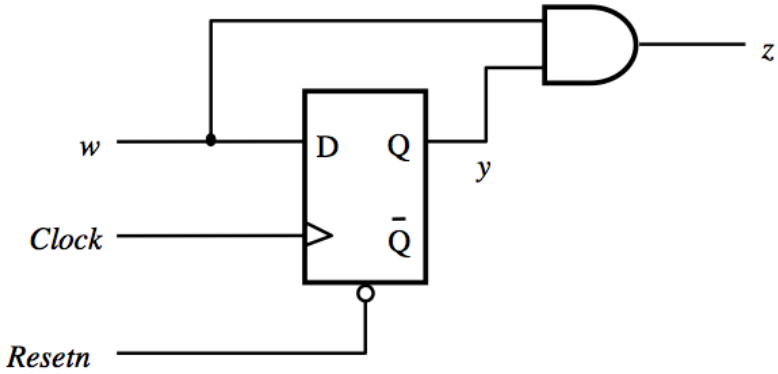
Moore


W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

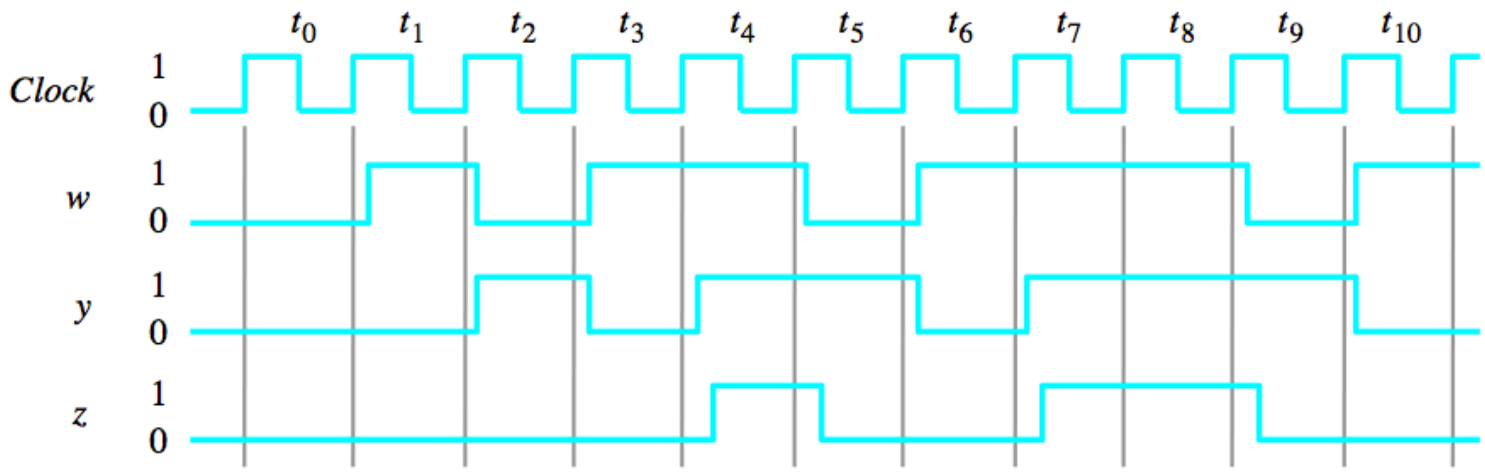

w
D
Q
y
z
D
Q
Z
Clock
Resetn

Mealy

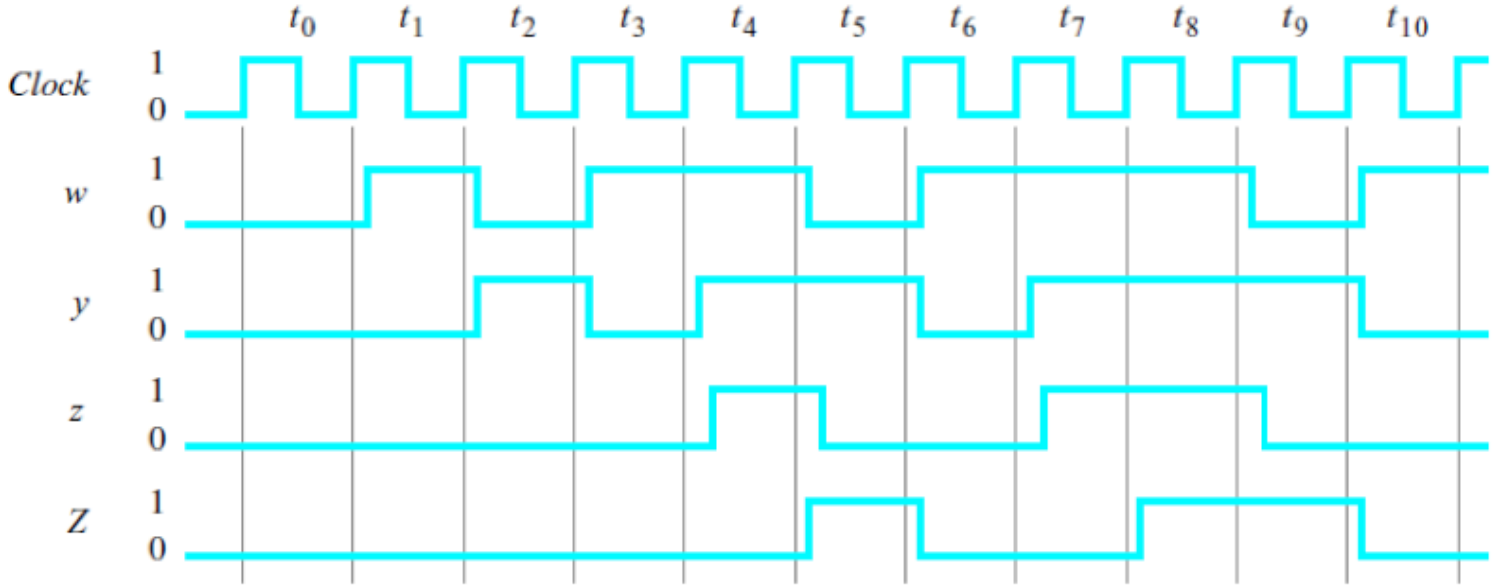

W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock


w
D
Q
y
z
Clock
Resetn

Mealy

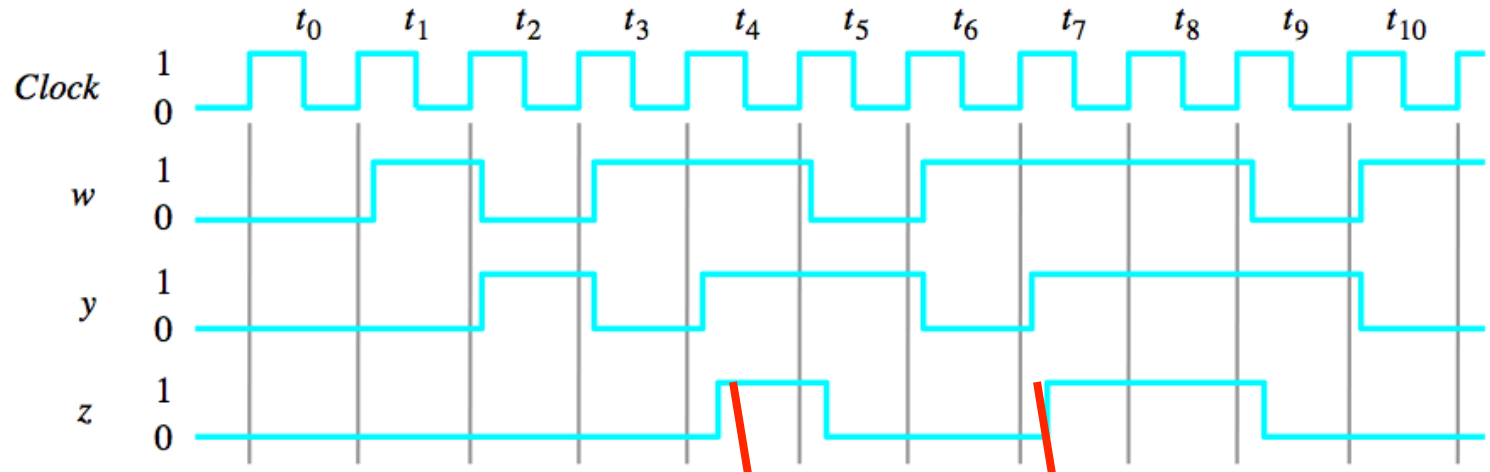

t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10}
Clock
w
y
z
1
0

Moore

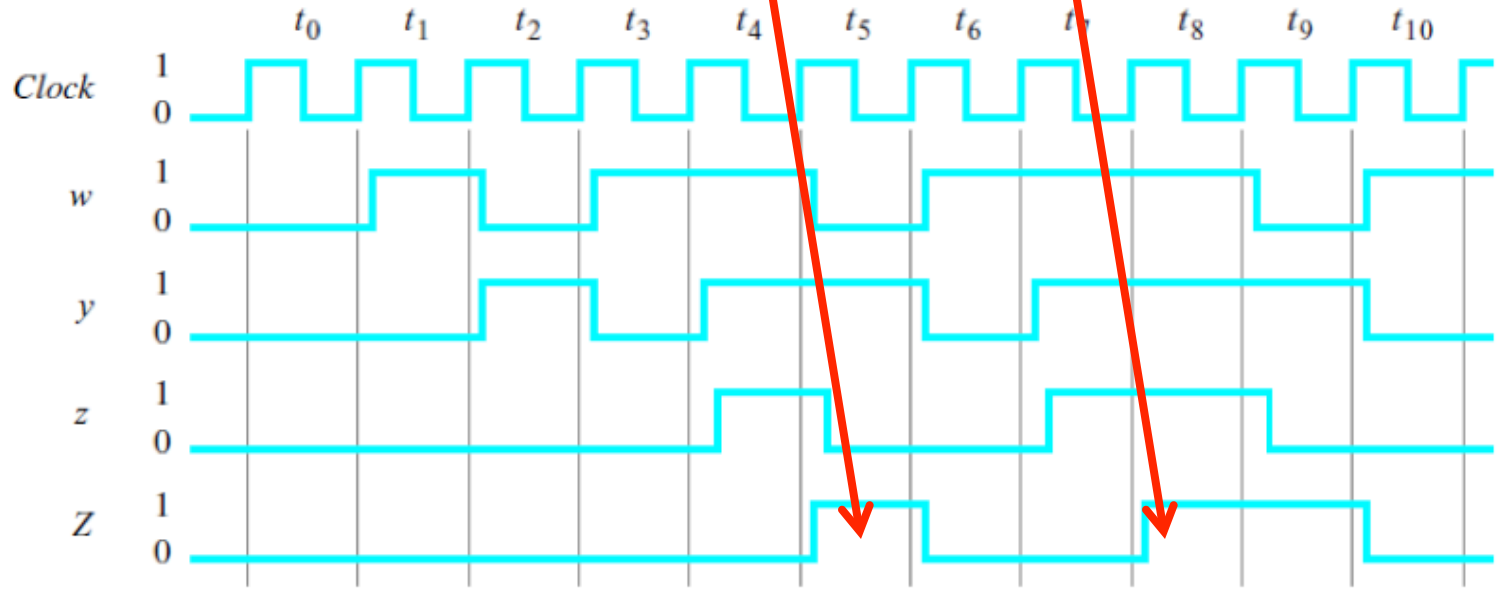

t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10}
Clock
w
y
z
Z
1
0

Notice that the output of the Moore machine is delayed by one clock cycle

Mealy



Moore



Questions?

THE END