



CprE 281: Digital Logic

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TA for Cpr E 281

<http://www.ece.iastate.edu/~alexs/classes/>

T Flip-Flops & JK Flip-Flops

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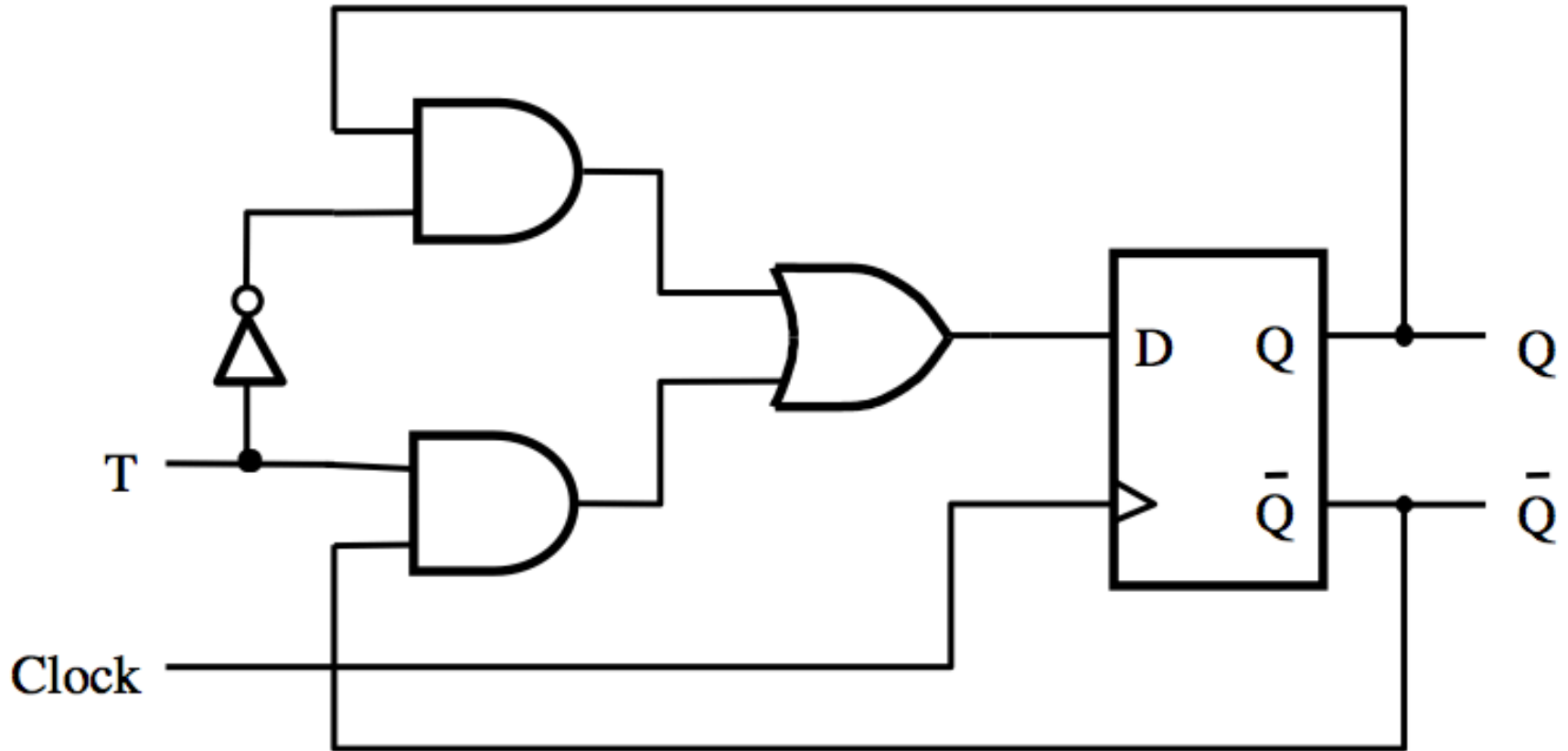
T Flip-Flop

Motivation

A slight modification of the D flip-flop that can be used for some nice applications.

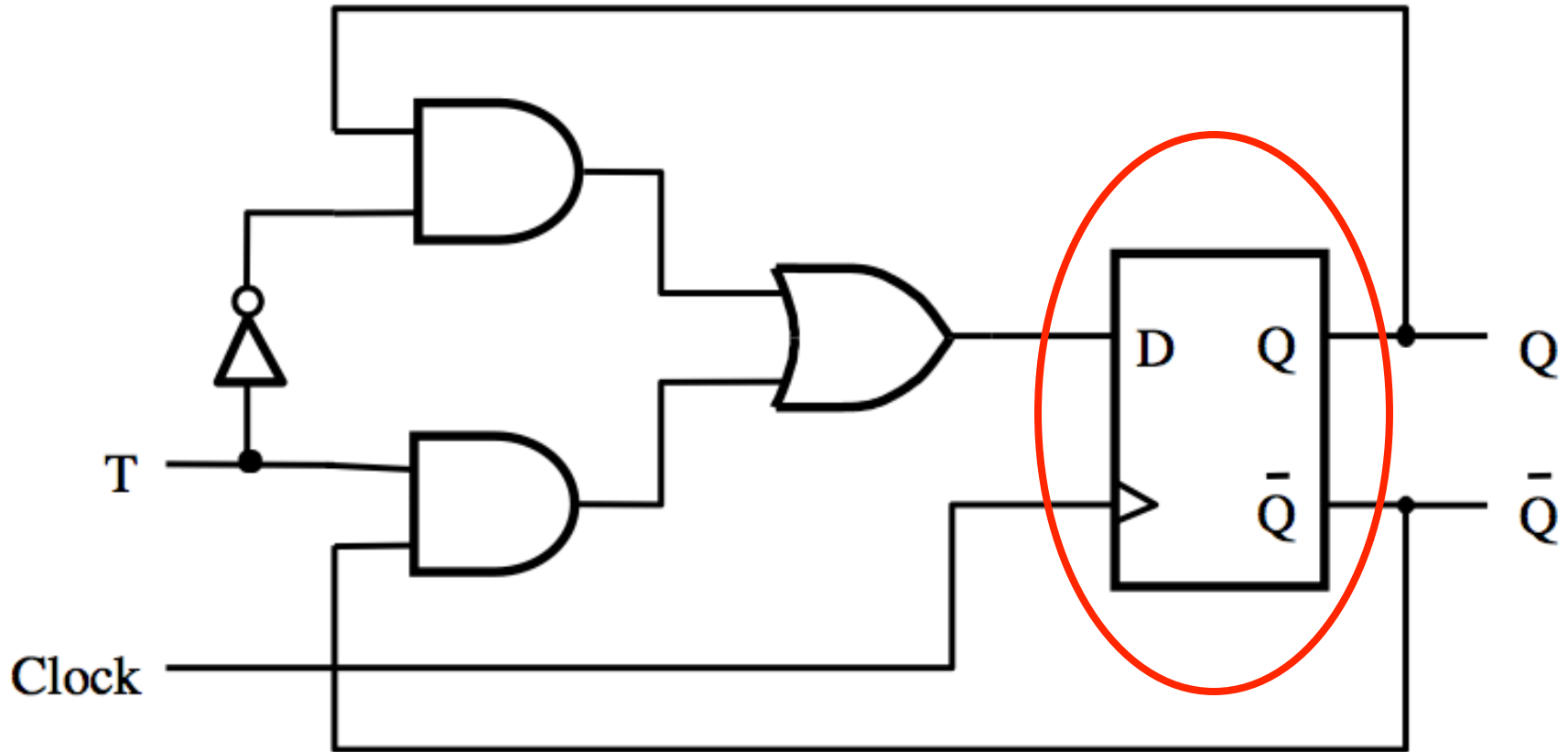
In this case, T stands for Toggle.

T Flip-Flop



[Figure 5.15a from the textbook]

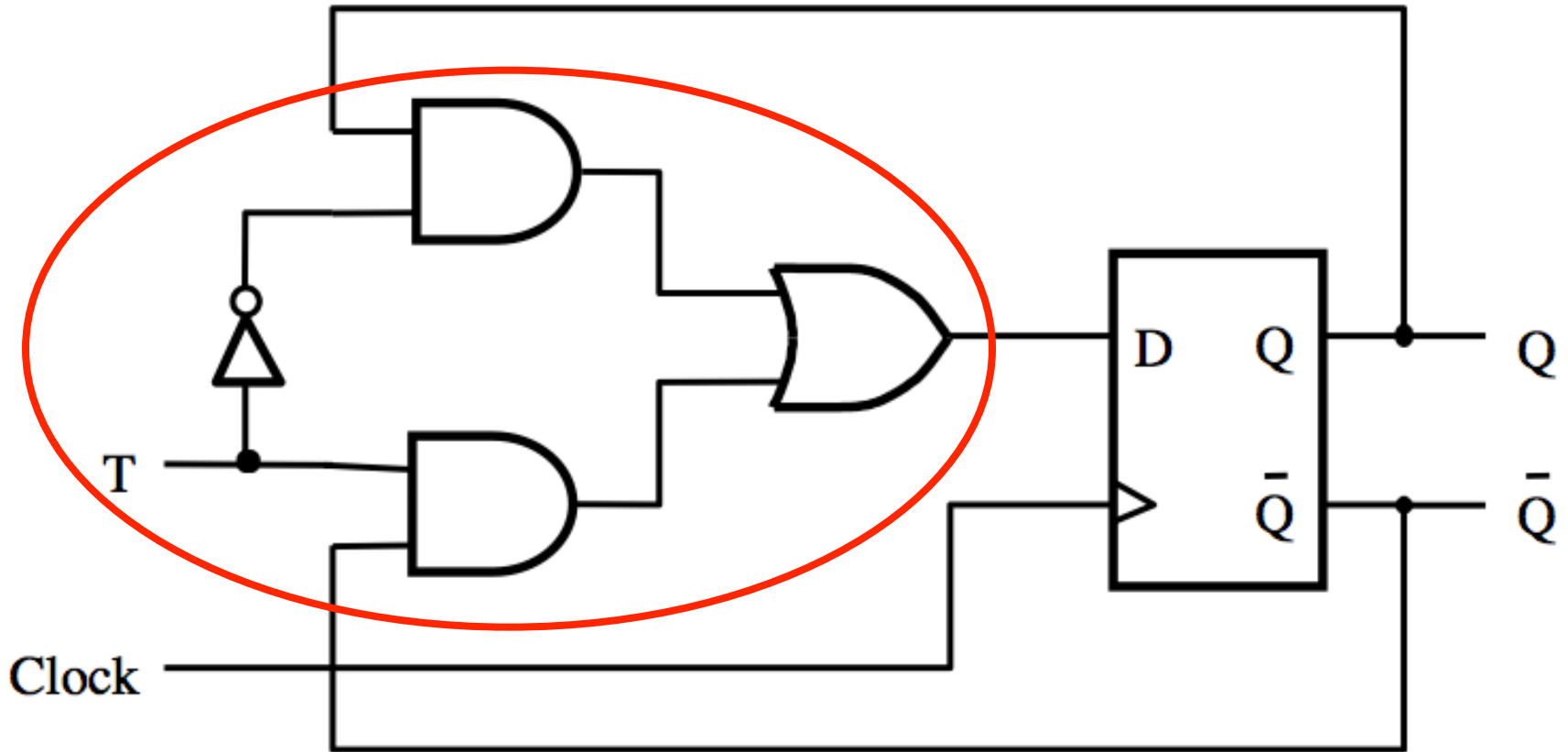
T Flip-Flop



Positive-edge-triggered
D Flip-Flop

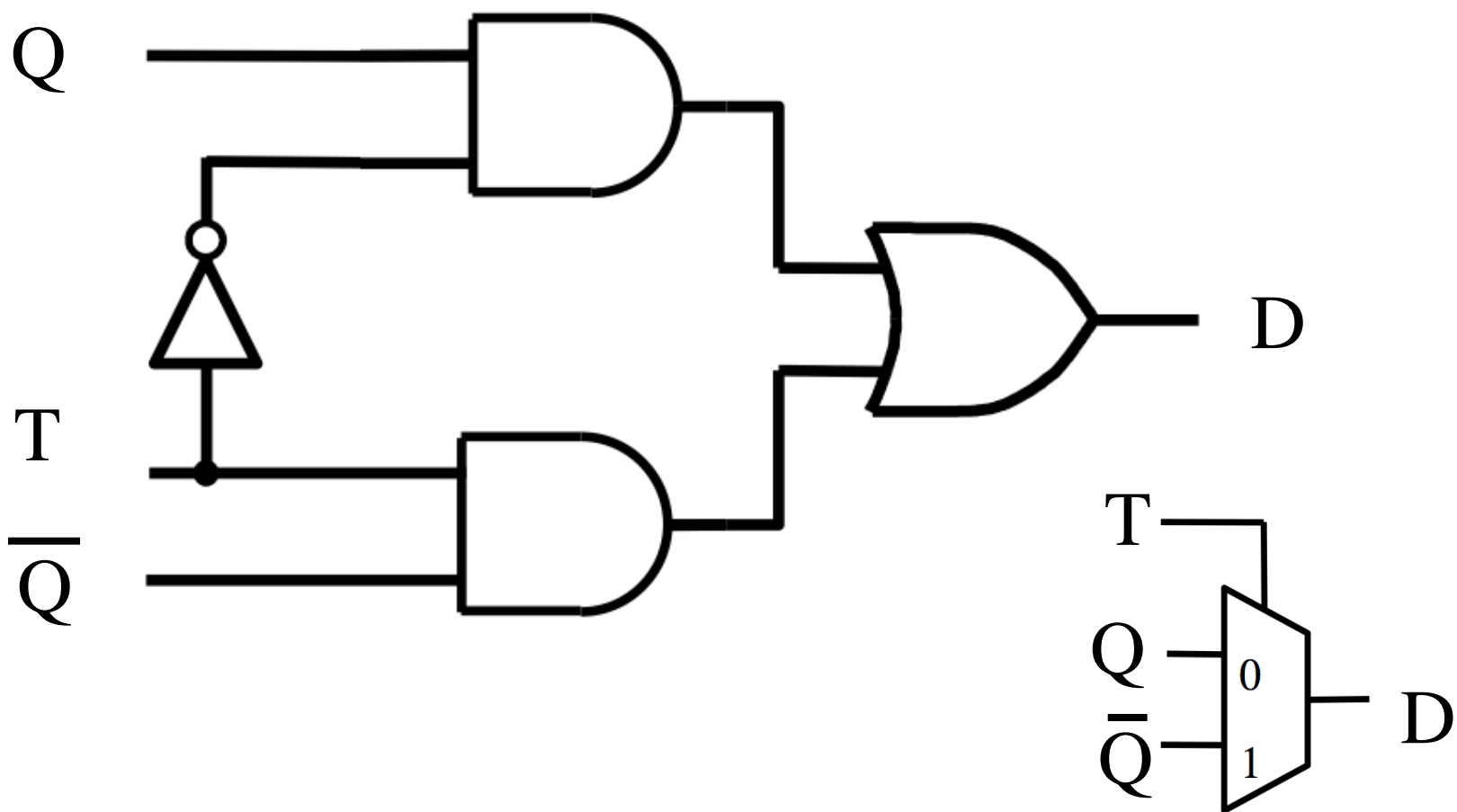
[Figure 5.15a from the textbook]

T Flip-Flop

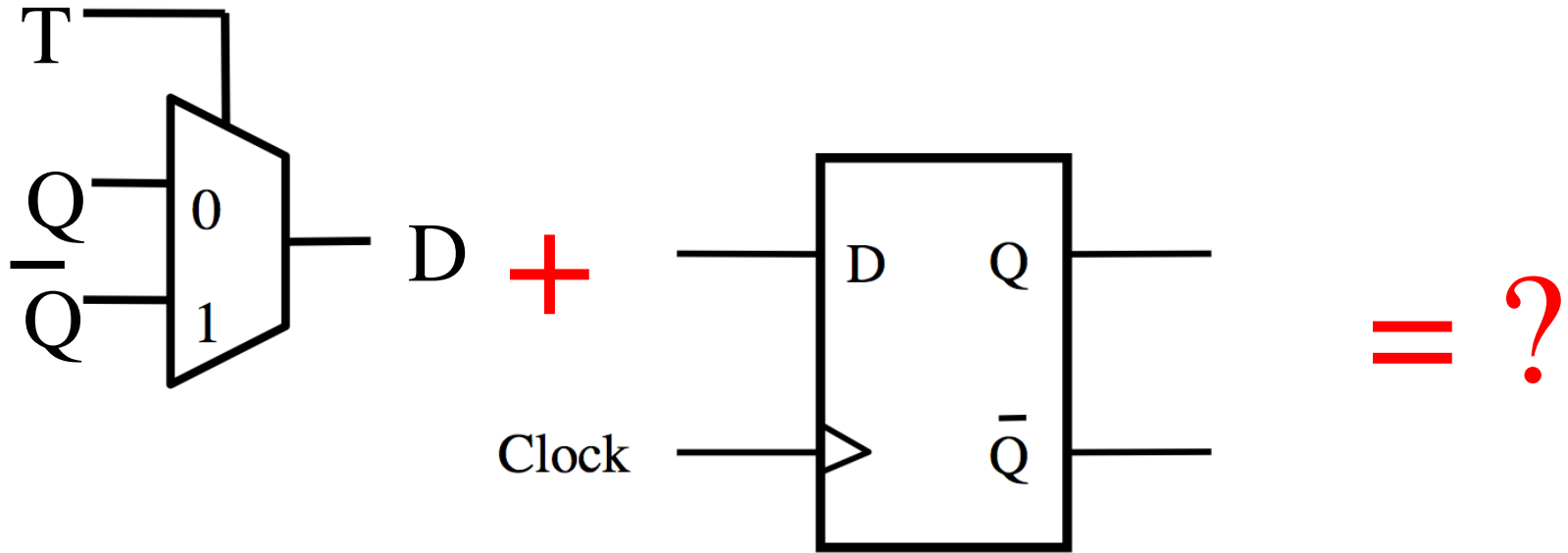


What is this?

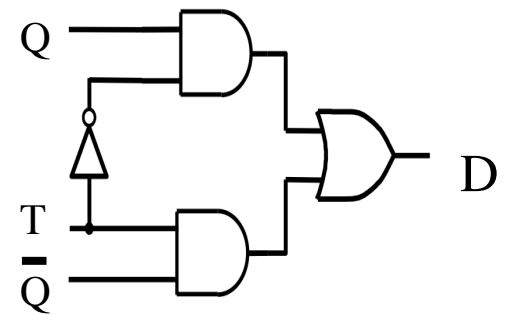
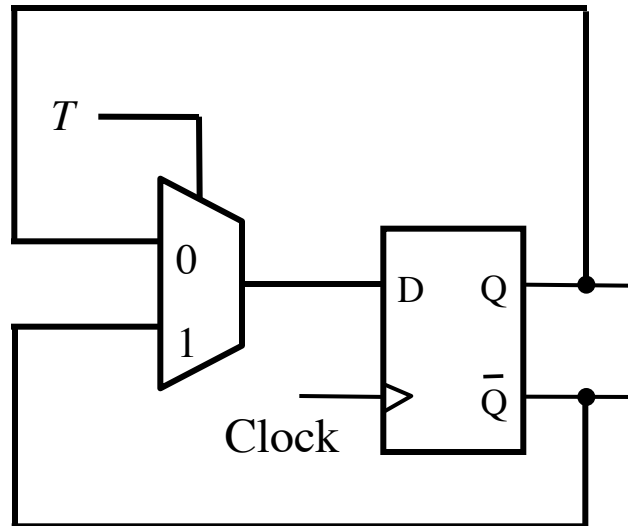
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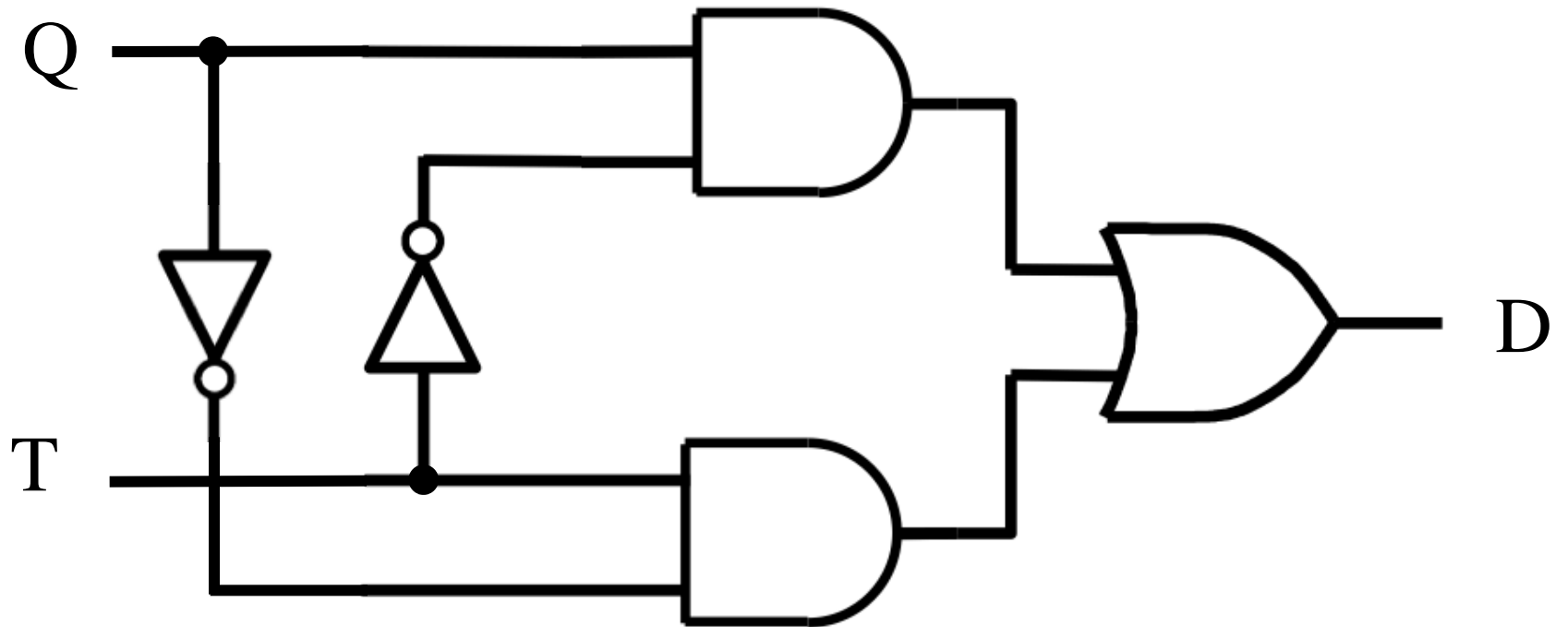
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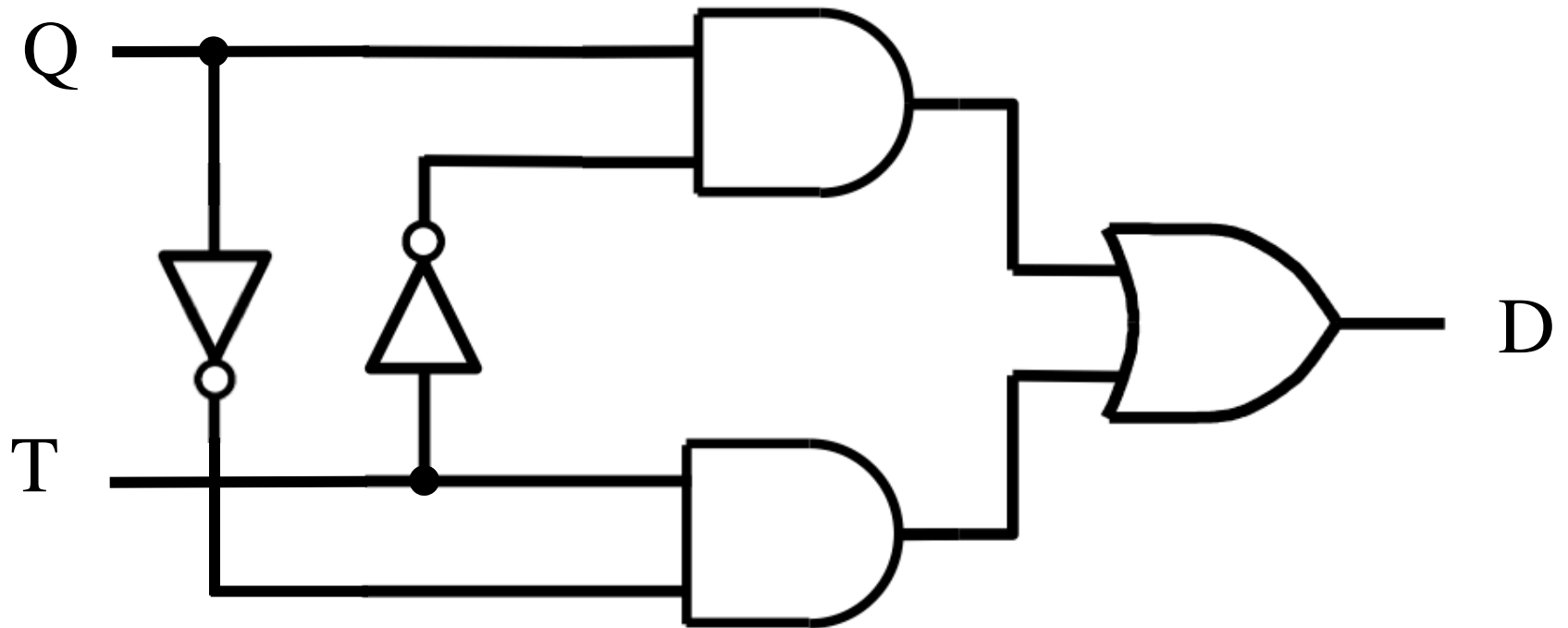
T Flip-Flop



What is this?

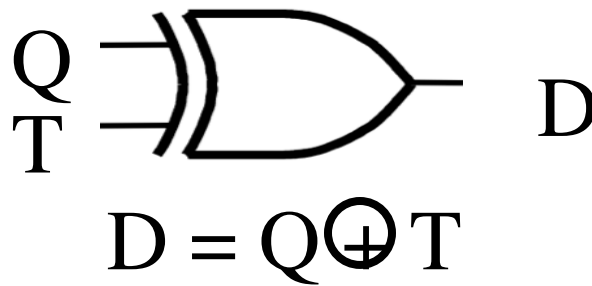
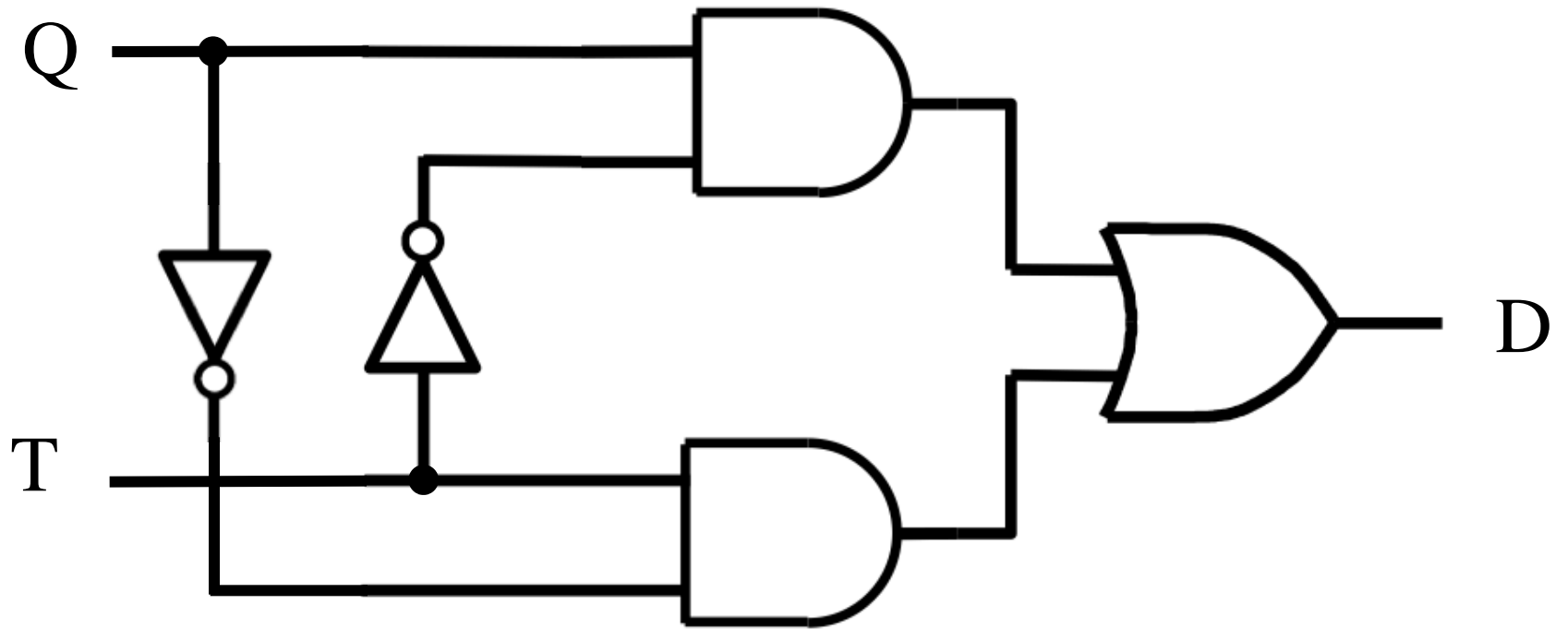


What is this?



$$D = \overline{Q}T + Q\overline{T}$$

What is this?

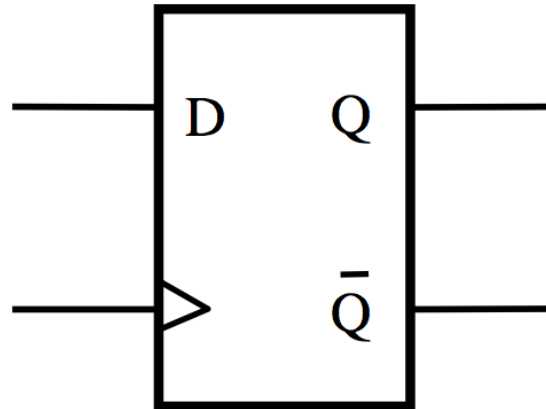


$$D = Q \oplus T$$

What is this?

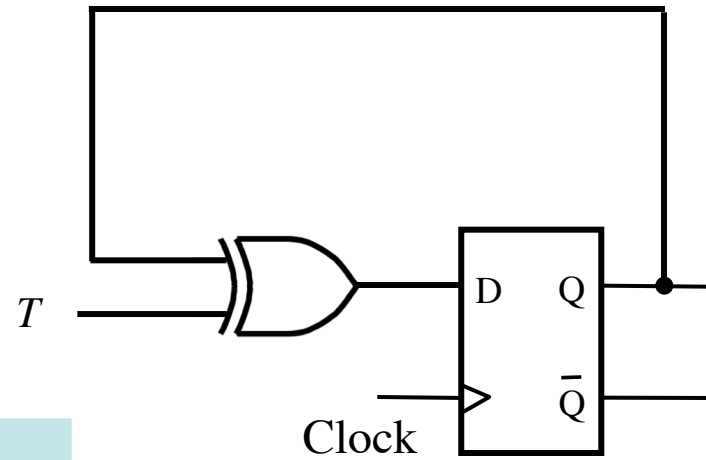


+
Clock



= ?

T Flip-Flop



T	Q	D	
0	0	0	Q
0	1	1	
1	0	1	Q'
1	1	0	

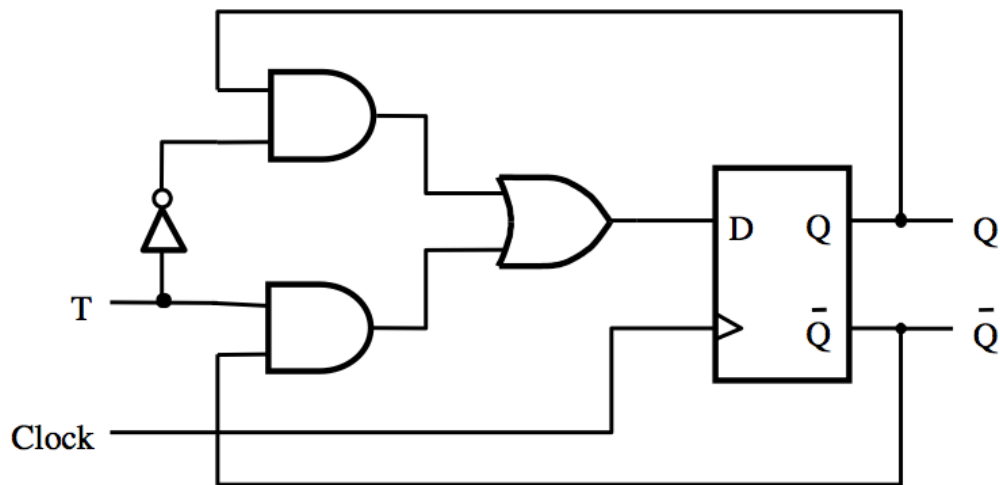
T Flip-Flop (How it Works)

If $T=0$ then it stays in its current state

If $T=1$ then it reverses its current state

In other words the circuit “toggles” its state when $T=1$. This is why it is called T flip-flop.

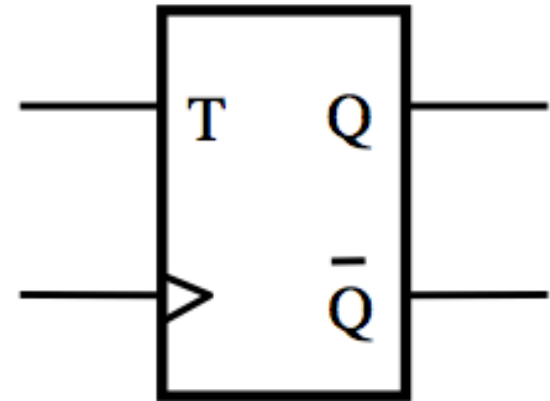
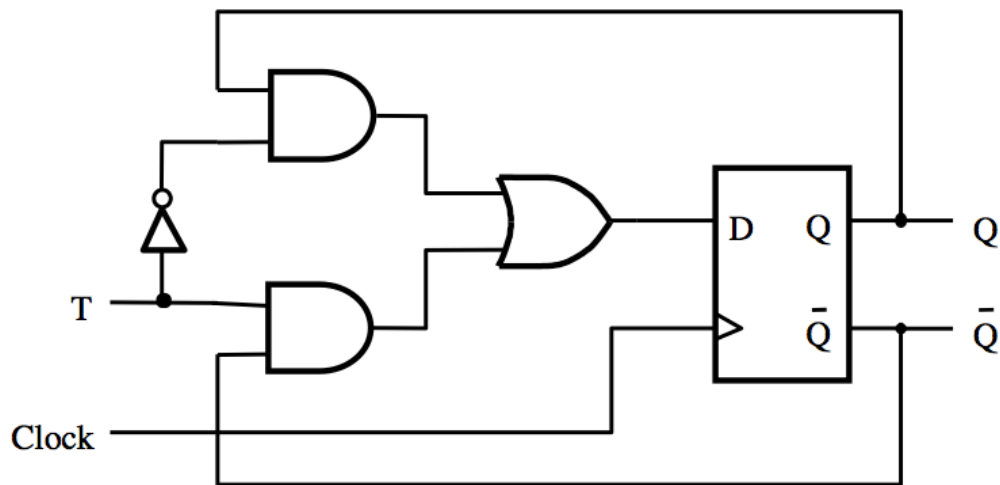
T Flip-Flop (circuit and truth table)



T	$Q(t+1)$
0	$Q(t)$
1	$\bar{Q}(t)$

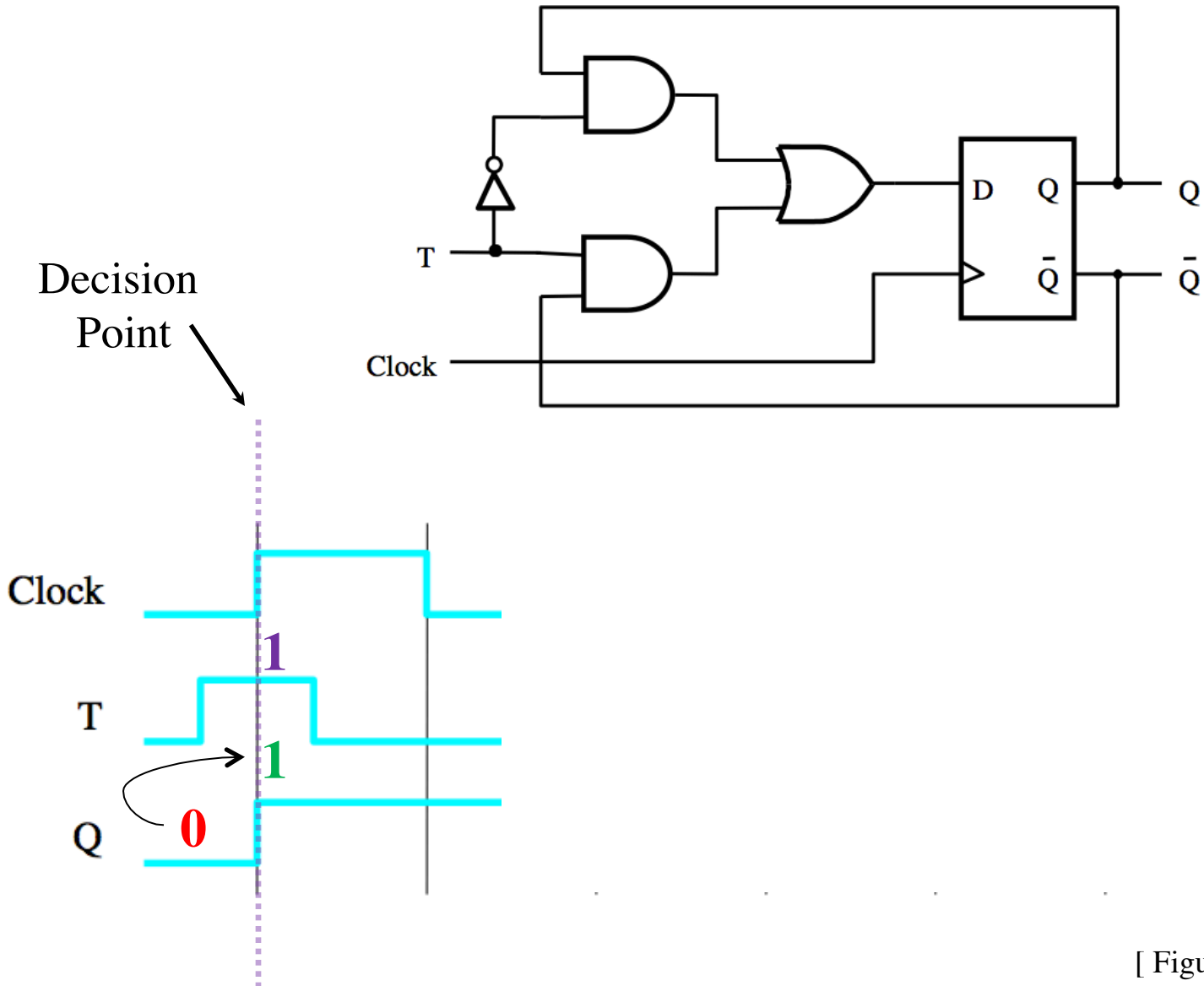
[Figure 5.15a,b from the textbook]

T Flip-Flop (circuit and graphical symbol)



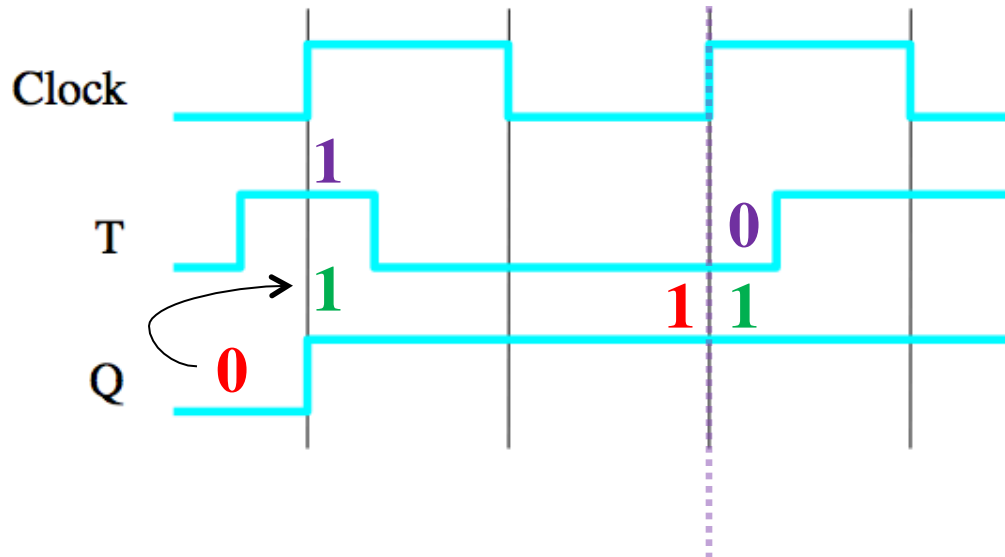
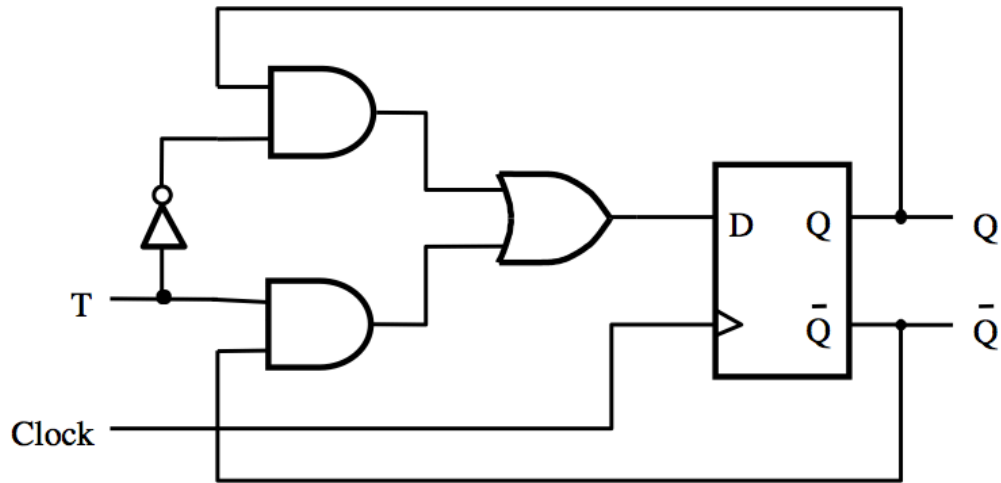
[Figure 5.15a,c from the textbook]

T Flip-Flop (Timing Diagram)



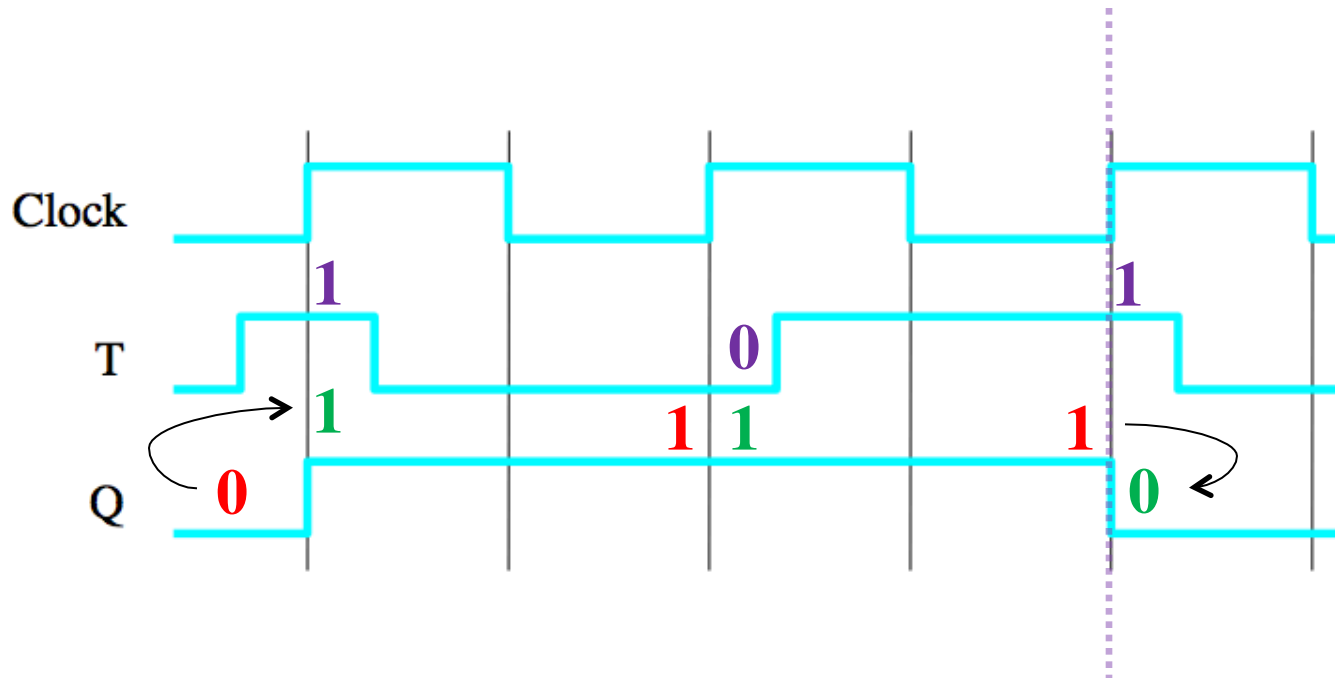
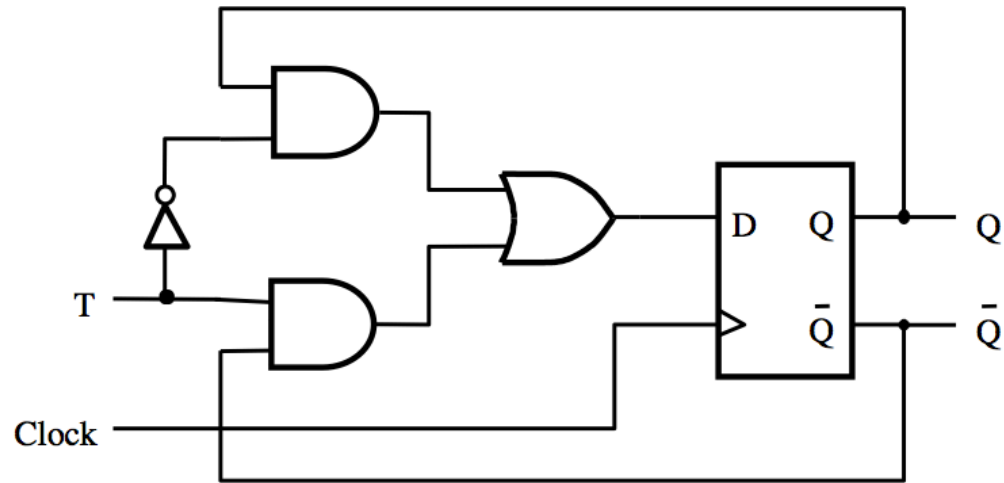
[Figure 5.15d from the textbook]

T Flip-Flop (Timing Diagram)



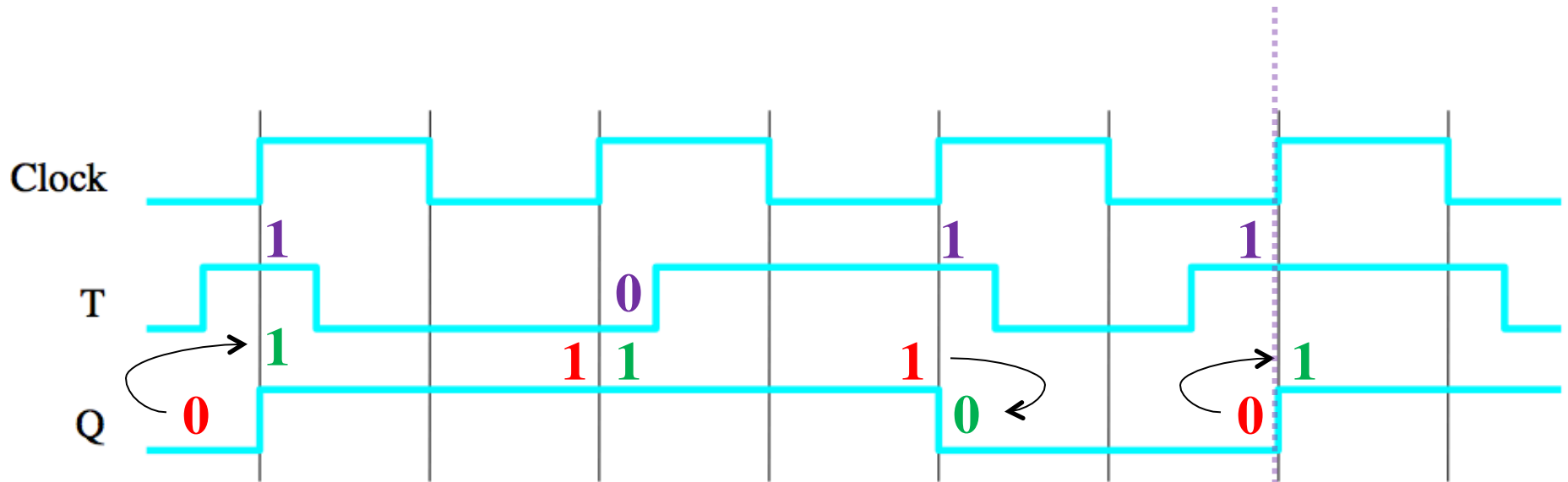
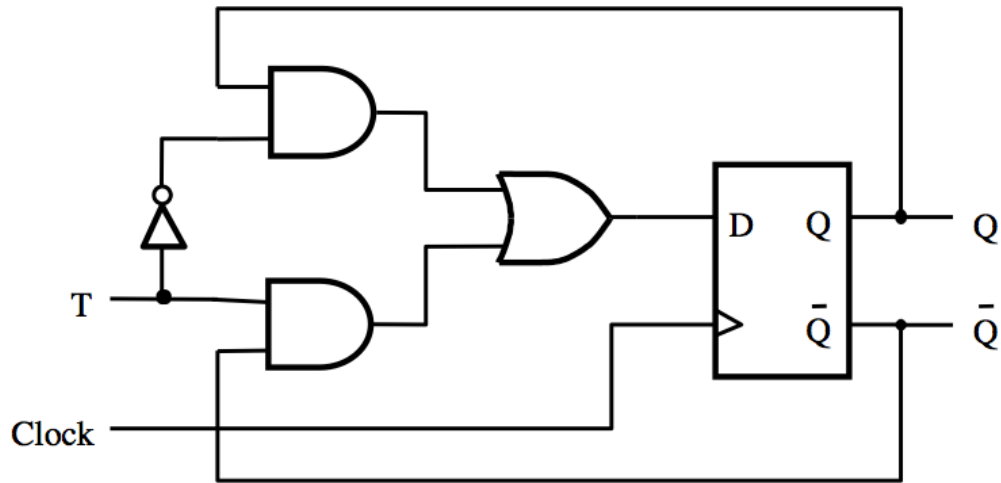
[Figure 5.15d from the textbook]

T Flip-Flop (Timing Diagram)



[Figure 5.15d from the textbook]

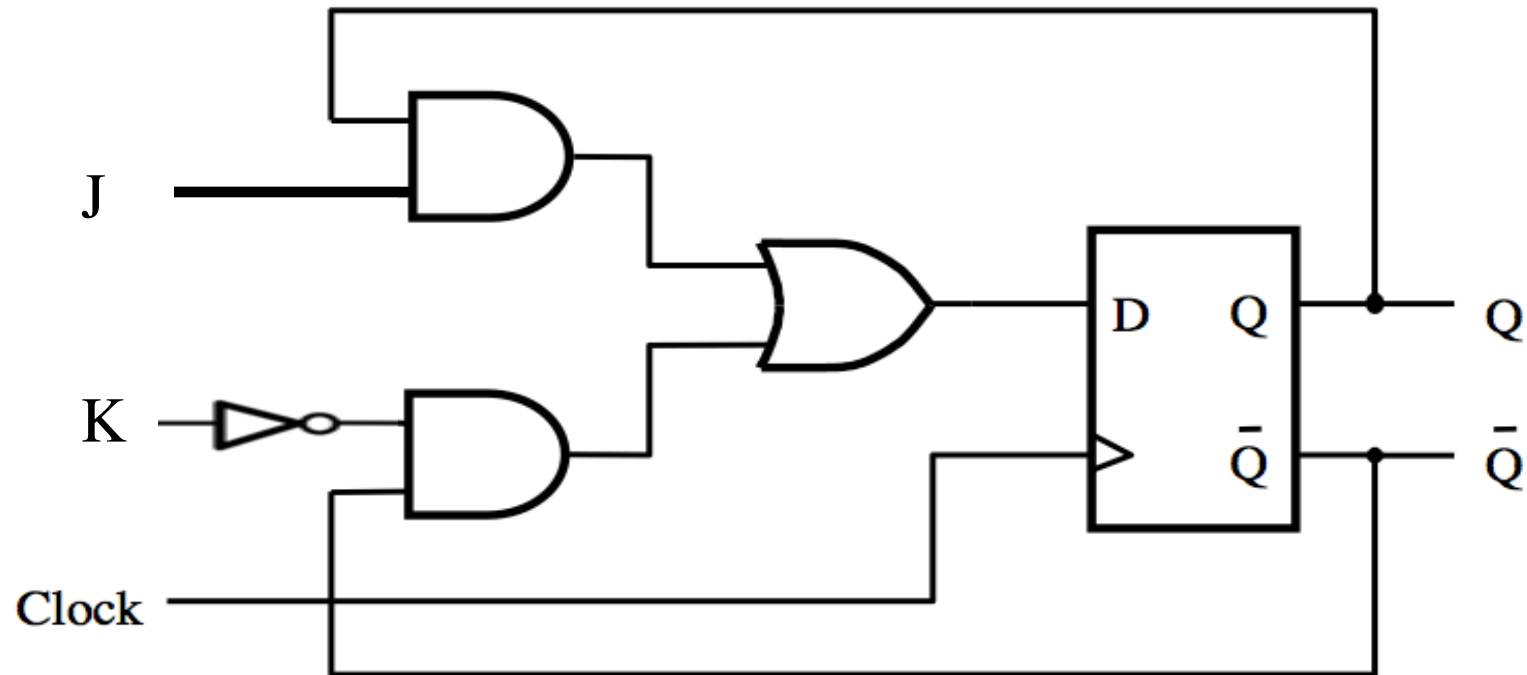
T Flip-Flop (Timing Diagram)



[Figure 5.15d from the textbook]

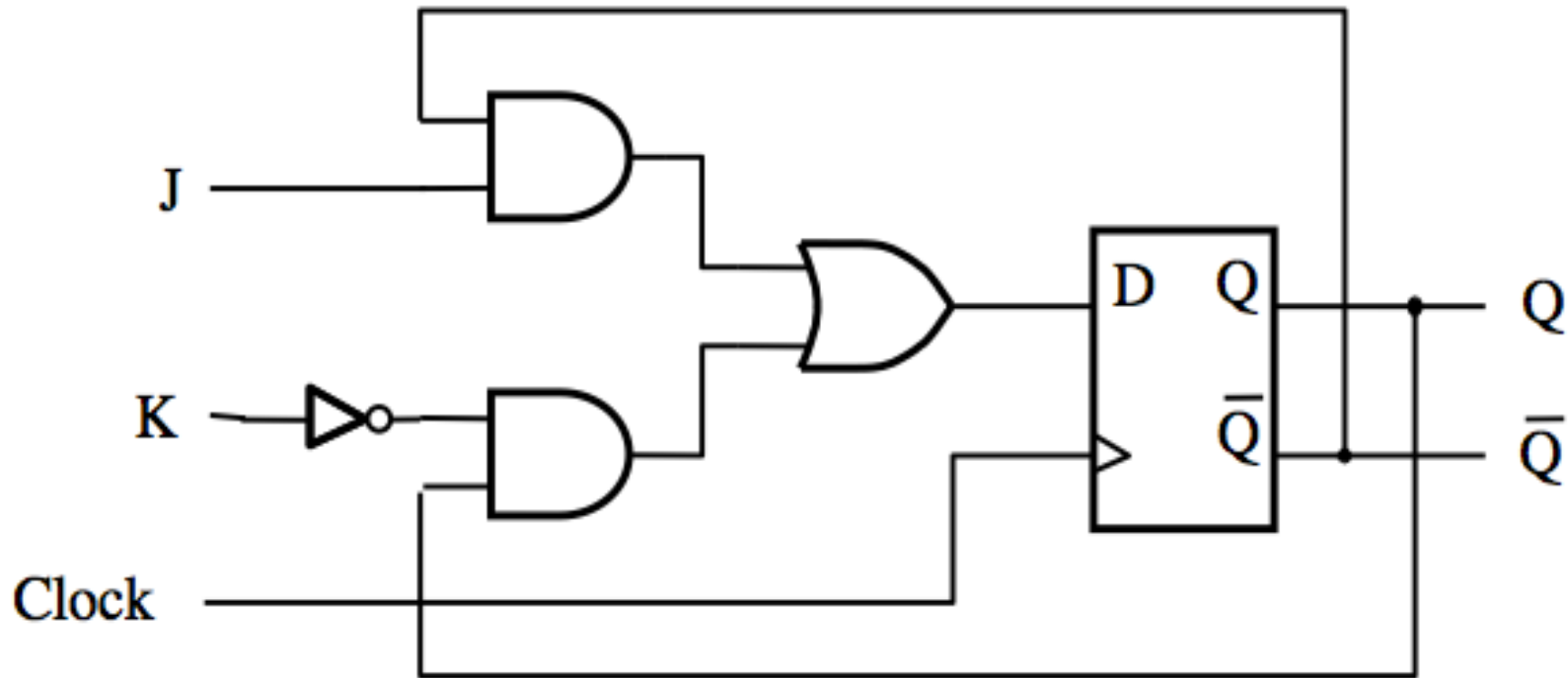
JK Flip-Flop

T Flip-Flop



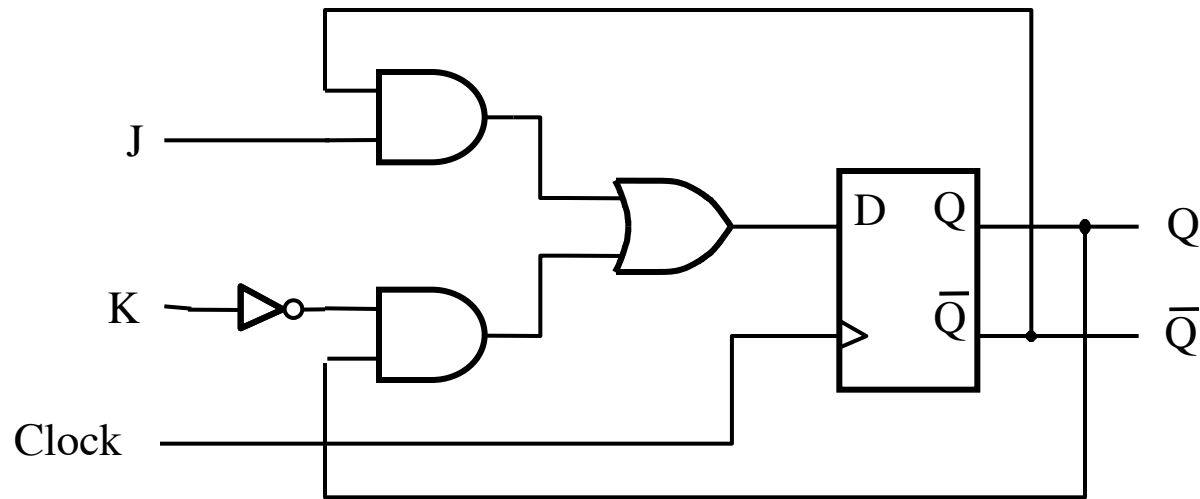
[Figure 5.16a from the textbook]

JK Flip-Flop



$$D = \bar{J}\bar{Q} + \bar{K}Q$$

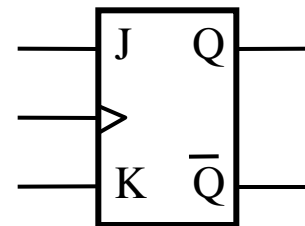
JK Flip-Flop



(a) Circuit

J	K	$Q(t+1)$	
0	0	$Q(t)$	Hold
0	1	0	Set
1	0	1	Reset
1	1	$\bar{Q}(t)$	Toggle

(b) Truth table



(c) Graphical symbol

JK Flip-Flop (How it Works)

A versatile circuit that can be used both as a SR flip-flop and as a T flip flop

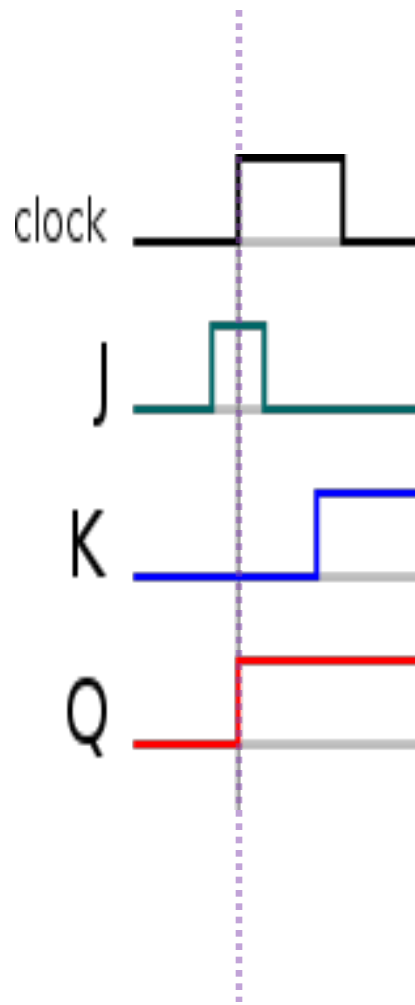
If $J=0$ and $S=0$ it stays in the same state

Just like SR It can be set and reset

$J=S$ and $K=R$

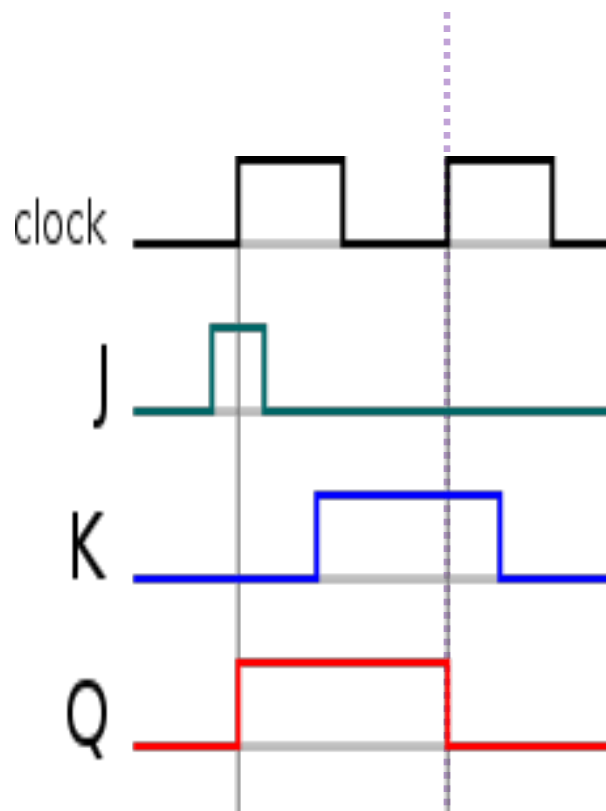
If $J=K=1$ then it behaves as a T flip-flop

JK Flip-Flop (How it Works)



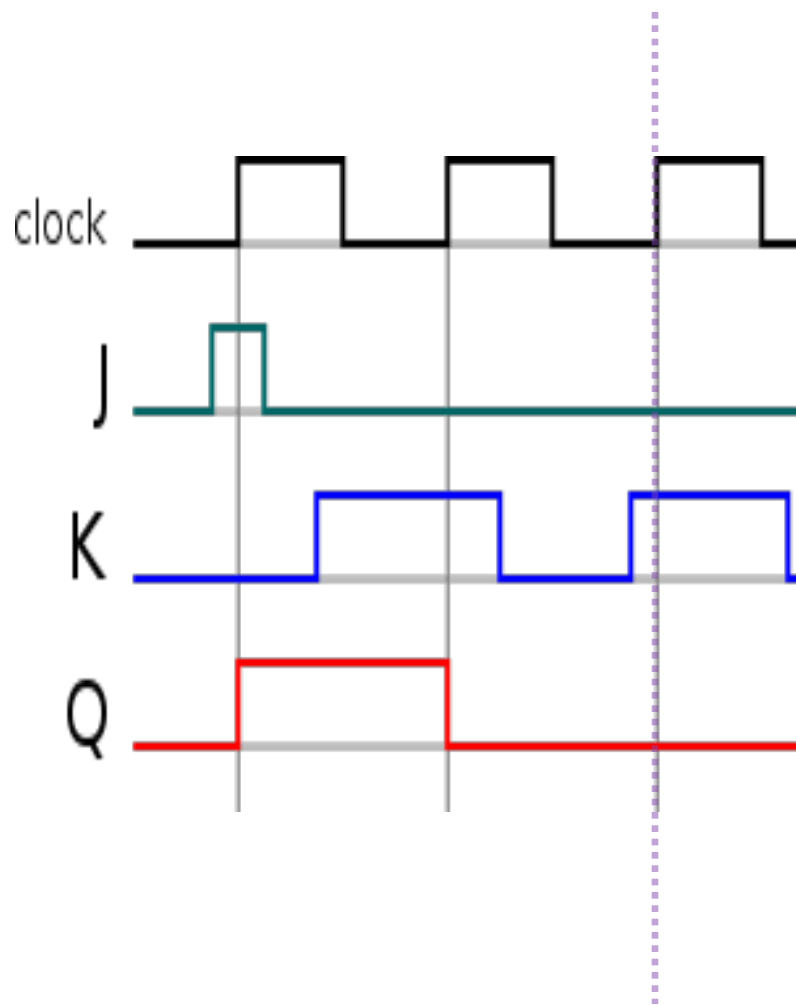
J	K	Q(t+1)
0	0	Q(t) Hold
0	1	0 Set
1	0	1 Reset
1	1	$\bar{Q}(t)$ Toggle

JK Flip-Flop (How it Works)



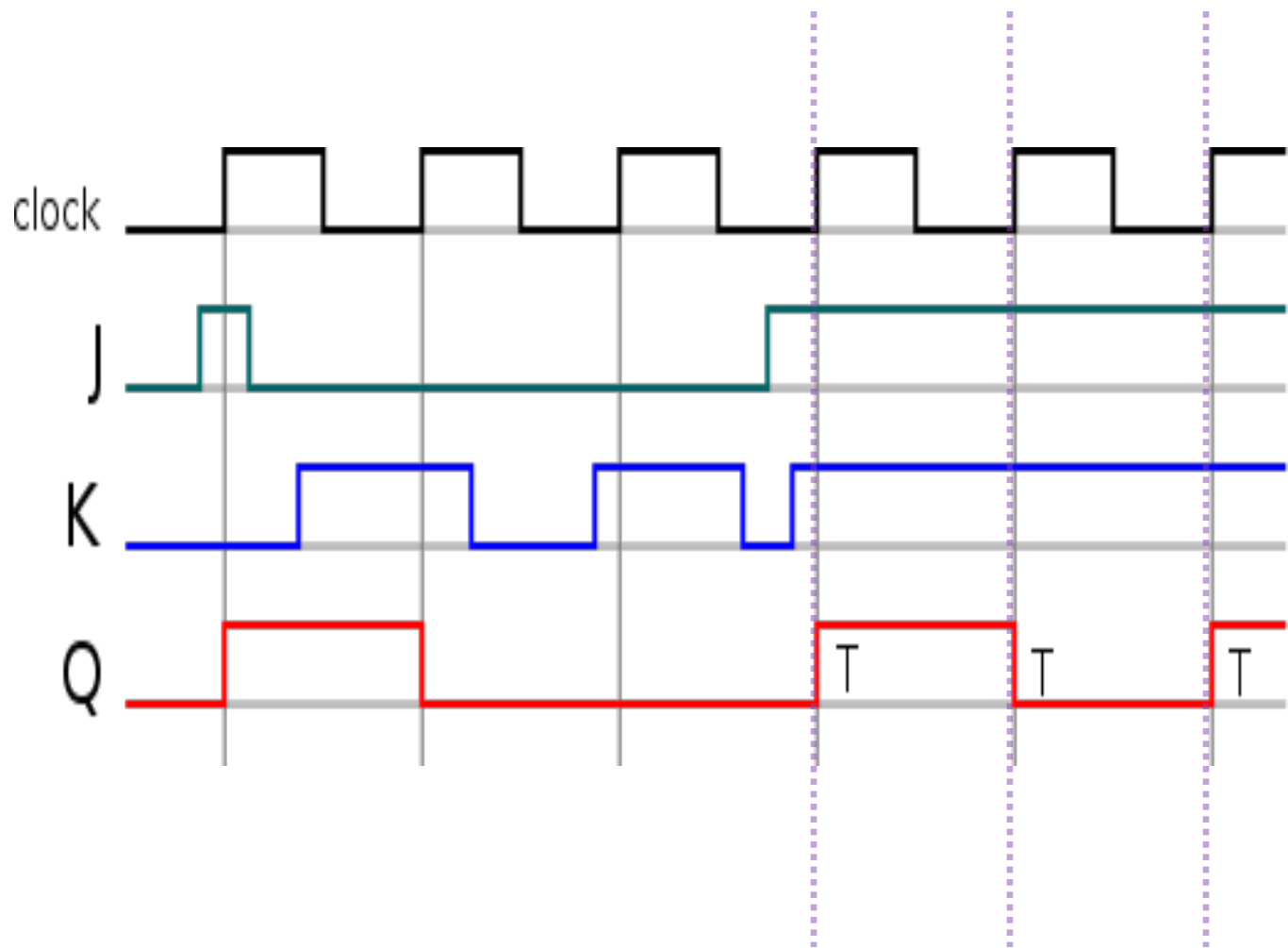
J	K	Q(t+1)
0	0	Q(t) Hold
0	1	0 Set
1	0	1 Reset
1	1	$\bar{Q}(t)$ Toggle

JK Flip-Flop (How it Works)



J	K	Q(t+1)
0	0	Q(t) Hold
0	1	0 Set
1	0	1 Reset
1	1	$\bar{Q}(t)$ Toggle

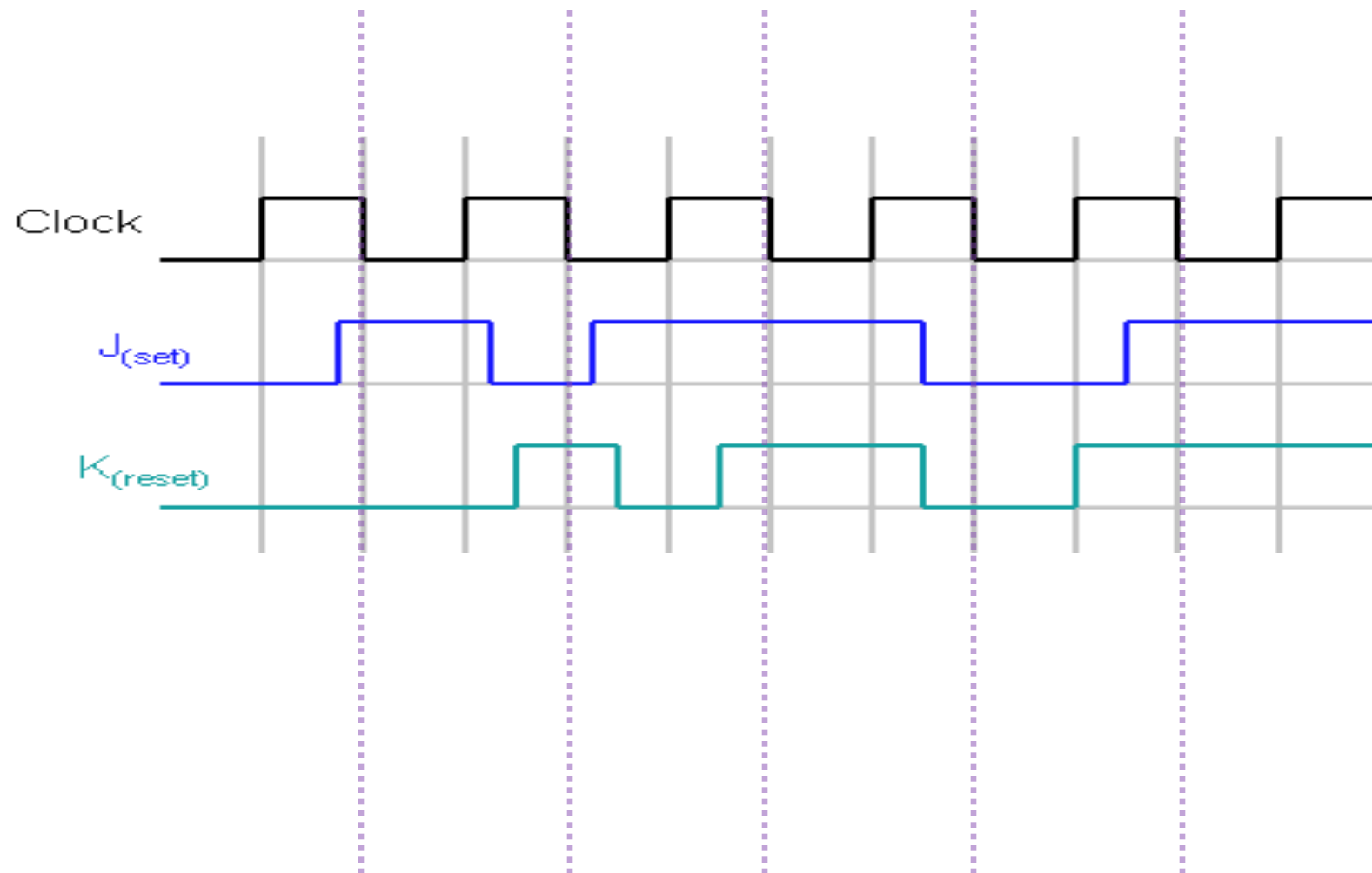
JK Flip-Flop (How it Works)



J	K	Q(t+1)
0	0	Q(t) Hold
0	1	0 Set
1	0	1 Reset
1	1	$\bar{Q}(t)$ Toggle

Questions?

Draw the wave form of Q for a (-ve edge) JK flip-flop



THE END