CprE 281: Digital Logic
Midterm 2: Friday Oct 30, 2015

Student Name: **Student ID Number:**

Lab Section:	**Mon 9-12(N)**	**Mon 12-3(P)**	**Mon 5-8(R)**	**Tue 11-2(U)**
(circle one)	**Tue 2-5(M)**	**Wed 8-11(J)**	**Wed 6-9(Y)**	**Thur 11-2(Q)**
	Thur 2-5(L)	**Thur 5-8(K)**	**Fri 11-2(G)**	

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name and student ID number. TRUE / FALSE

(b) Any Boolean function can be implemented using only T flip-flops. TRUE / FALSE

(c) A D flip-flop can be implemented with a JK flip-flop and one NOT gate. TRUE / FALSE

(d) A T flip-flop can be implemented with a D flip-flop and one XOR gate. TRUE / FALSE

(e) A T flip-flop can be implemented with a D flip-flop and a 2-to-1 multiplexer.TRUE / FALSE

(f) A T flip-flop can be implemented with only 6 NAND gates. TRUE / FALSE

(g) A 1-to-2 decoder can be implemented with only one NOT gate. TRUE / FALSE

(h) Any function f(x,y,z) can be realized with a 3-to-8 decoder and one OR gate. TRUE / FALSE

(i) The total delay through a full-adder is 2 gate delays. TRUE / FALSE

(j) In a carry-lookahead adder all sum signals are generated after 3 gate delays. TRUE / FALSE

2. Minimization using a K-map (5p)
Draw the K-map for the function f(a,b,c,d) = Σ m(1,3,4,6,11,13,14). Then use the K-map to derive the minimized SOP expression for the function f.

3.Binary Addition and Subtraction (5 x 3p each = 15p)

Convert the following integers into binary numbers and perform the addition or subtraction using 2's complement if necessary. Write your answers and all intermediary steps to the right of each problem. Use 5-bit numbers for all problems and indicate if any bits need to be ignored.

```
  (+11)
+
  (+ 2)
-------
```

```
  (+9)
+
  (-6)
------
```

```
  (- 4)
+
  (+10)
-------
```

```
  (-2)
-
  (-5)
-------
```

```
  (-12)
-
  (- 8)
-------
```

4. Number Conversions (3p + 4p + 4p + 4p = 15p)

(a) Convert 196_{10} to binary:

(b) Convert the following 32-bit float number (in IEEE 754 format) to decimal

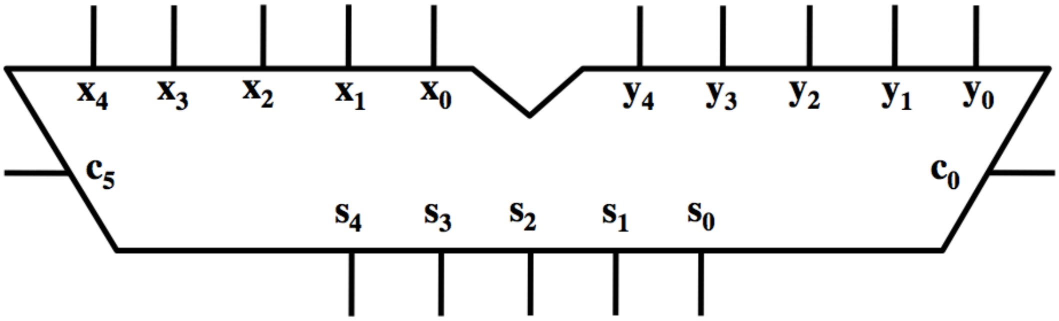
1 1 0 0 0 0 1 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

(c) Write down the 32-bit floating point representation (in IEEE 754 format) for 0110_2

(d) Write down the 32-bit floating point representation (in IEEE 754 format) for -7_{10}

5. Implementation using an Adder (7p + 3p = 10p)

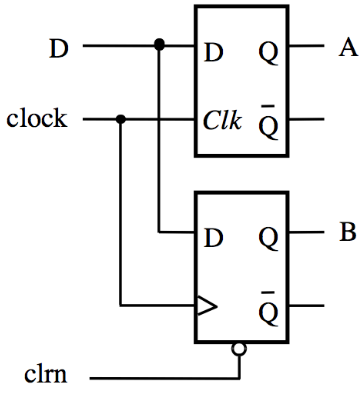
a) Let A (a3, a2, a1, a0) be a 4-bit number, let B (b5, b4, b3, b2, b1, b0) be a 6-bit number, and let s be a 1-bit number. Draw a circuit that uses the 5-bit adder shown below and any other basic logic gates (ANDs, ORs, or NOTs) to compute the value of B as follows: if s=0 then B = 4A+1; if s=1 then B=2A. Clearly label all inputs and outputs. (7p)

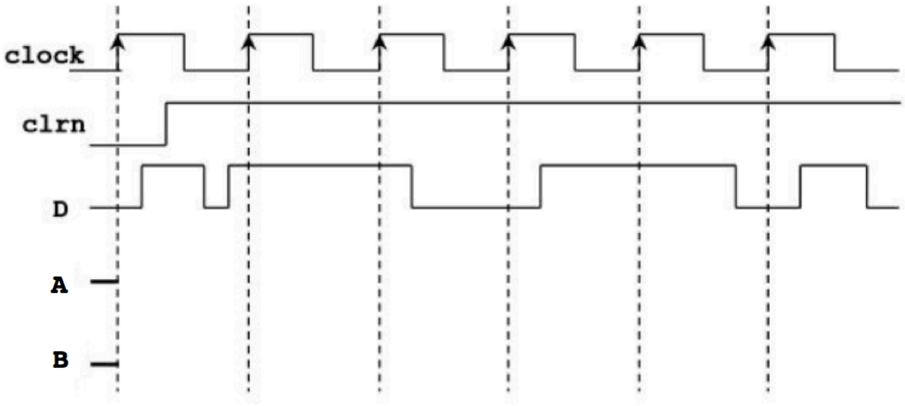


b) Explain your solution. (3p)

6. Flip-Flops and Timing Diagrams (5p + 10p = 15p)

a) **Complete the timing diagram for the circuit shown below. Assume that both A and B are initially equal to zero. (5p)**





b) **Draw the complete circuit diagram for a positive-edge-triggered JK flip-flop using <u>only</u> standard logic gates (ANDs, ORs, NOTs, NANDs, or NORs). You are not allowed to use any other high-level components in this problem. (10p)**

7. Multiplexers (2p + 8p = 10p)

a) **Draw the truth table for the function** $\mathbf{f = x\,y + x\,z + y\,z}$ **(2p)**

b) **Implement this function using <u>only</u> 2-to-1 multiplexers and <u>no other logic gates</u>. Assume that the signals X, Y, and Z are available <u>only</u> in their non-inverted form. (8p)**

8. Comparator (3p + 7p = 10p)

A 1-bit comparator is a circuit that has two inputs (A and B) and three outputs (L, E, and G). Each of the two inputs is a 1-bit number. The first output, L, is equal to one if A<B and zero otherwise. The second output, E, is equal to one if A=B and zero otherwise. Finally, the third output, G, is equal to one if A>B and zero otherwise.

a) Draw the truth table for the 1-bit comparator. (3p)

b) Draw the circuit for this comparator using only 4-to-1 multiplexers and no other gates. (7p)

9. More Multiplexers (2p + 8p = 10p)

a) Draw the truth table for the function $f = \overline{A}\,C + B\,C\,D + \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}.$ (2p)

b) Implement the function f using only 2-to-1 multiplexers and no other gates. You can assume that the variables are available in both inverted and and non-inverted form. Clearly label all inputs, pins, and outputs of your circuit. (8p)

10. Product Check (3 x 5p = 15p)

The goal is to design a circuit that takes a 3-bit number A(a2, a1, a0) and a 2-bit number B(b1, b0) and sets the output F to 1 if $B \neq 0$ and $A=2B$. Otherwise $F=0$.

a) **Complete the truth table for the function F.** (5p)

b) **Write the logic expression for F in canonical SOP form.** (5p)

c) **Implement a circuit for F using one 8-to-1 multiplexer and some basic logic gates. Please label clearly all inputs, output, and pins of your circuit.** (5p)

a2	a1	a0	b1	b0	F
0	0	0	0	0	
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	
1	0	0	0	0	
1	0	0	0	1	
1	0	0	1	0	
1	0	0	1	1	
1	0	1	0	0	
1	0	1	0	1	
1	0	1	1	0	
1	0	1	1	1	
1	1	0	0	0	
1	1	0	0	1	
1	1	0	1	0	
1	1	0	1	1	
1	1	1	0	0	
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	

11. Implement a Multiplexer (10p + 5p = 15p)

a) Implement a 8-to-1 multiplexer using only one 2-to-4 decoder (without enable input) and any additional N-input AND, OR, or NOT gates. Label all inputs, pins, and outputs. (10p)

b) Explain your solution. How many additional gates are required? (5p)

Question	**Max**	**Score**
1. True/False	10	
2. K-Map Minimization	5	
3. Addition/Subtraction	15	
4. Number Conversions	15	
5. Adder Implementation	10	
6. Flip-Flops	15	
7. Multiplexers	10	
8. Comparator	10	
9. More Multiplexers	10	
10. Product Check	15	
11. Implement a Multiplexer	15	
TOTAL:	130	