CprE 281: Digital Logic
Midterm 1: Friday Sep 25, 2015

Student Name: **Student ID Number:**

Lab Section:	**Mon 9-12(N)**	**Mon 12-3(P)**	**Mon 5-8(R)**	**Tue 11-2(U)**
(circle one)	**Tue 2-5(M)**	**Wed 8-11(J)**	**Wed 6-9(Y)**	**Thur 11-2(Q)**
	Thur 2-5(L)	**Thur 5-8(K)**	**Fri 11-2(G)**	

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name, student ID, and lab section. TRUE / (FALSE)

(b) It is possible to build a NOT gate with a 2-to-1 multiplexer. (TRUE) / FALSE

(c) It is possible to build an AND gate with a 2-to-1 multiplexer. (TRUE) / FALSE

(d) It is not possible to build an OR gate with a 2-to-1 multiplexer. TRUE / (FALSE)

(e) It is possible to build a NOT gate with an XOR gate. (TRUE) / FALSE

(f) $\overline{a} \cdot \overline{c} + a \cdot c = 1$ TRUE / (FALSE)

(g) $x \cdot y + \overline{x} = x + y$ TRUE / (FALSE)

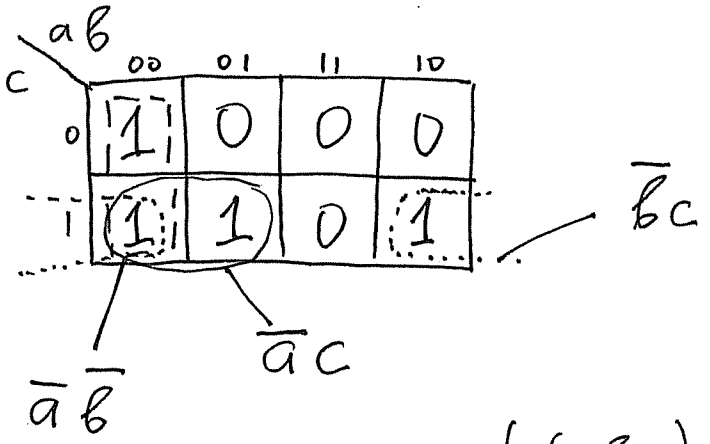
(h) $(\overline{x} + y) \cdot (\overline{x} + \overline{y}) = \overline{x}$ (TRUE) / FALSE

(i) $x + (y + z) = (x + y) + z$ (TRUE) / FALSE

(j) $\overline{x + y} = \overline{x} + \overline{y}$ TRUE / (FALSE)

2. Three-Variable K-map (5p)

Draw the K-map and derive the minimum SOP expression for **f(a,b,c) = Σm (0, 1, 3, 5)**



$f(a,b,c) = \overline{a}\,\overline{b} + \overline{a}c + \overline{b}c$

3.Truth Tables (5p + 10p = 15p)

(a) Draw the truth table for the Boolean function that has the following K-map

Z \ XY	00	01	11	10
0	0	0	1	0
1	0	1	1	1

X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(b) Draw the truth table for the Boolean function $F = \overline{A}\cdot\overline{C} + \overline{B}\cdot\overline{D} + C\cdot D$

A	B	C	D	$\overline{A}\,\overline{C}$	$\overline{B}\,\overline{D}$	C D	F
0	0	0	0	1	1	0	1
0	0	0	1	1	0	0	1
0	0	1	0	0	1	0	1
0	0	1	1	0	0	1	1
0	1	0	0	1	0	0	1
0	1	0	1	1	0	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	0	1	1
1	0	0	0	0	1	0	1
1	0	0	1	0	0	0	0
1	0	1	0	0	1	0	1
1	0	1	1	0	0	1	1
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	1	1

4. Number Conversions (4 x 5p each = 20p)

(a) Convert 10011011_2 to decimal

$1\times2^7 + 0\times2^6 + 0\times2^5 + 1\times2^4 + 1\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0 =$

$128 + 0 + 0 + 16 + 8 + 0 + 2 + 1 = 155_{10}$

(b) Convert 178_{10} to binary

178 / 2 = 89 0
89 / 2 = 44 1
44 / 2 = 22 0
22 / 2 = 11 0
11 / 2 = 5 1
5 / 2 = 2 1
2 / 2 = 1 0
1 / 2 = 0 1

$178_{10} = 10110010_2$

(c) Convert 156_7 to octal:

$156_7 = 1\times7^2 + 5\times7^1 + 6\times7^0 = 49 + 35 + 6 = 90_{10}$

90 / 8 = 11 2
11 / 8 = 1 3
1 / 8 = 0 1

$156_7 = 132_8$

(d) Convert 6253_8 to hexadecimal

First convert to binary and then to hexadecimal

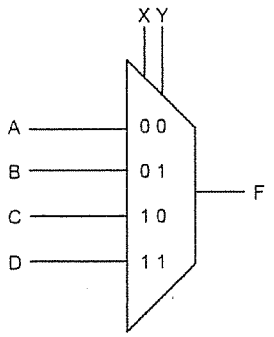
$6253_8 = 1100\,1010\,1011_2 = CAB_{16}$

C A B

5. Verilog Module (10p)

Write a Verilog module for the 4-to-1 multiplexer shown below.

Hint: $F = \overline{X}\,\overline{Y}\,A + \overline{X}\,Y\,B + X\,\overline{Y}\,C + X\,Y\,D$

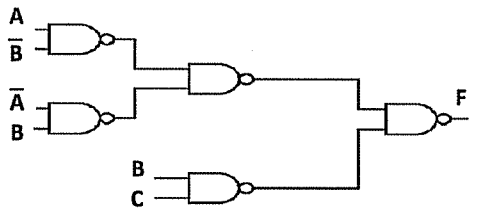



```
module mux_4_1(F, A, B, C, D, X, Y);
  input A, B, C, D, X, Y;
  output F;

  assign F = (~X&~Y&A)|(~X&Y&B)|(X&~Y&C)|(X&Y&D);
endmodule
```

6. Circuit to Circuit Conversion (3 x 5p = 15p)

(a) Write the expression for the function F given by this circuit (don't simplify it yet).



$$F = A\overline{B}\ \ \overline{A}B\ \ \overline{BC}$$

(b) Use the theorems of Boolean algebra to simplify the expression from part (a).

$$F = \overline{A\overline{B}\ \ \overline{A}B\ \ \overline{BC}} = \overline{A\overline{B}}\ \ \overline{\overline{A}B} + \overline{BC} \qquad \text{(De Morgan)}$$

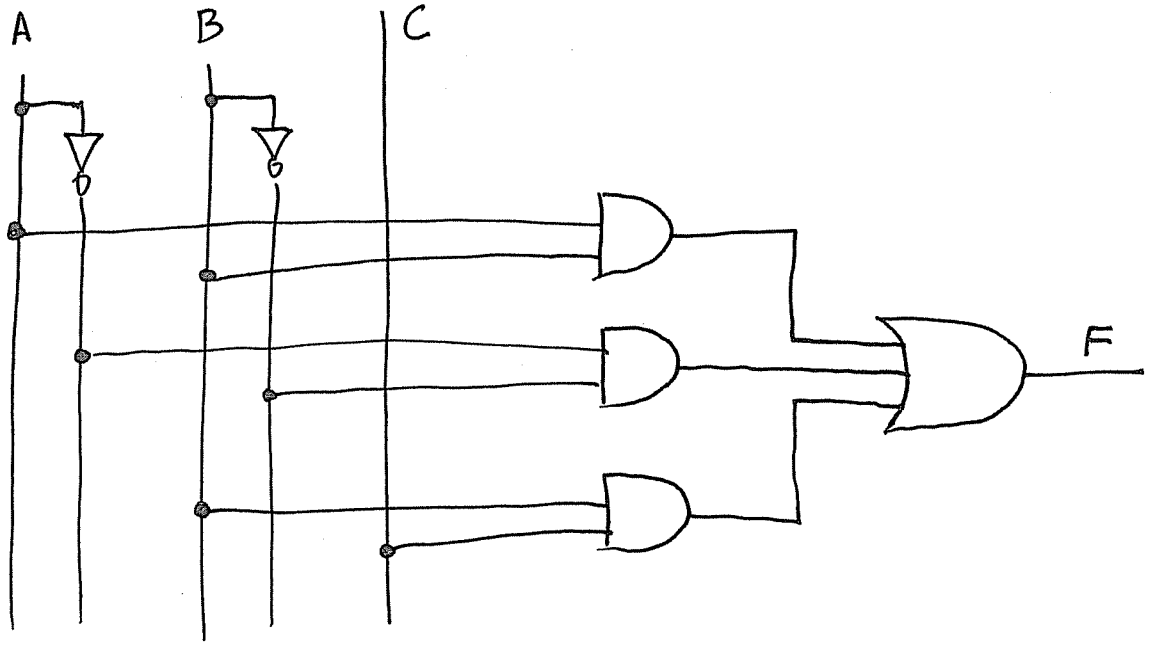
$$= \overline{A}\overline{\overline{B}}\ \ \overline{\overline{A}}\overline{B} + BC \qquad \text{(remove double negation)}$$

$$= (\overline{A} + B)(A + \overline{B}) + BC \qquad \text{(De Morgan)}$$

$$= \underbrace{\overline{A}A}_{0} + \overline{A}\overline{B} + BA + \underbrace{B\overline{B}}_{0} + BC$$

$$= AB + \overline{A}\overline{B} + BC$$

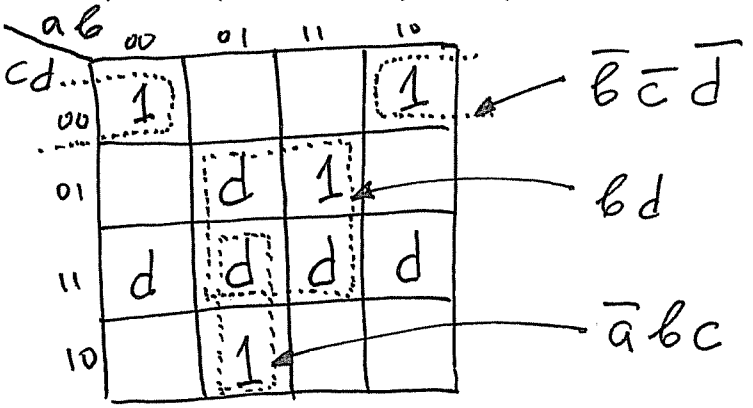
(c) Draw the circuit for your expression from part (b). Label all inputs and outputs.



7. Derive the minimum SOP expression using a K-map (3 x 5p = 15p)

(a) Draw the K-map for the following function

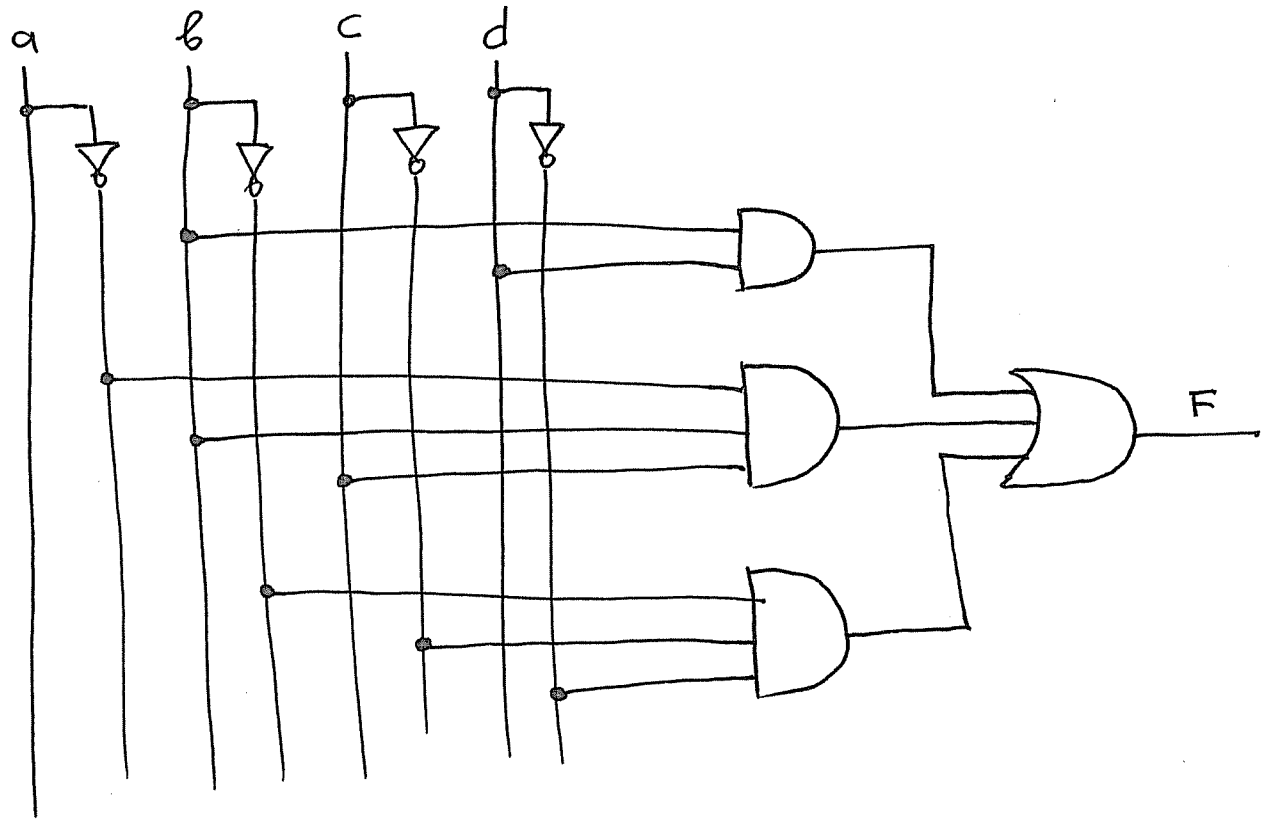
$$F(a,b,c,d)=\Sigma m(0, 6, 8, 13) + D(3, 5, 7, 11, 15)$$



(b) Use the K-map to derive the minimum-cost SOP expression for the function F.

$$F = b\bar{d} + \bar{a}bc + \bar{b}\bar{c}\bar{d}$$

(c) Draw the circuit diagram for the minimum expression from part (b).

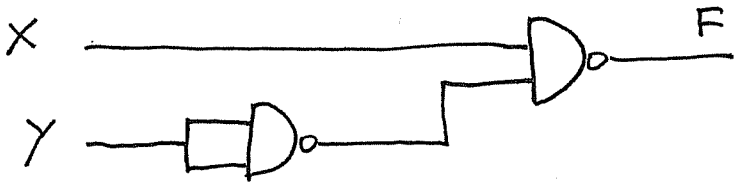


8. NAND/NOR Logic (5p + 5p = 10p)

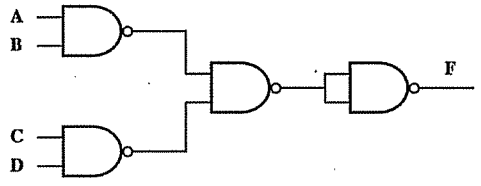
(a) Using only NAND gates, draw the logic circuit that corresponds to the truth table shown below. Hint: Start by writing and then modifying the expression for F.

X	Y	F
0	0	1
0	1	1
1	0	0
1	1	1

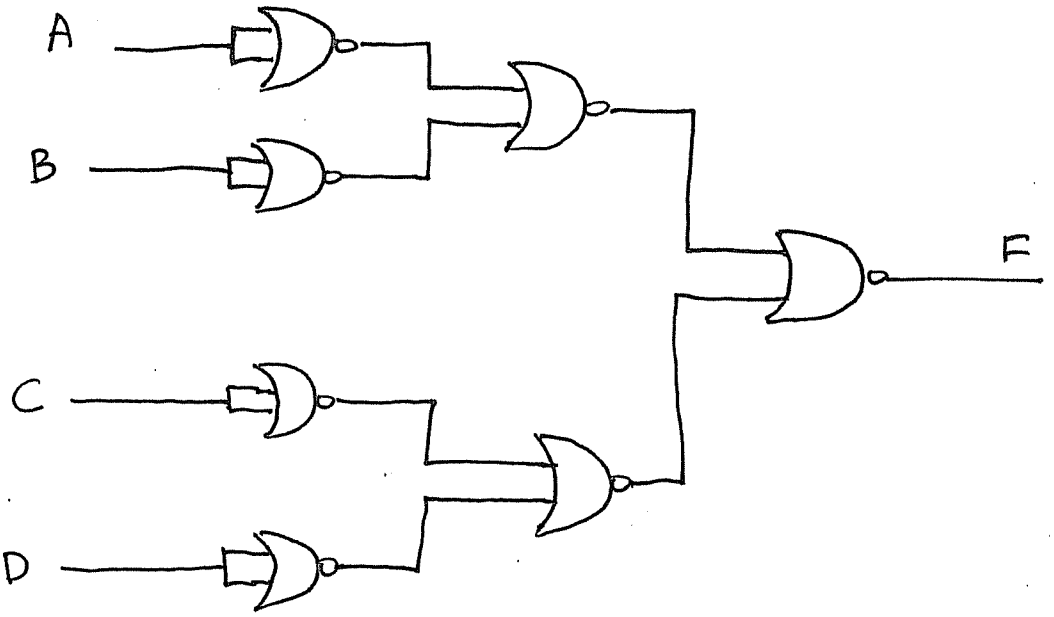
$$F = \overline{X} + Y = \overline{\overline{\overline{X} + Y}} = \overline{\overline{\overline{X}}\,\overline{Y}} = X\,\overline{Y}$$



(b) Redraw the following logic circuit using only NOR gates.



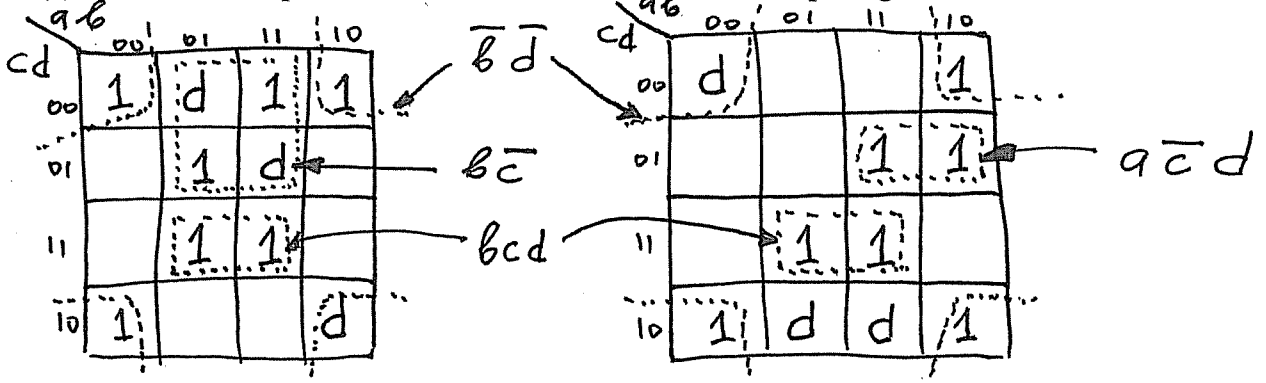
$$F = \overline{\overline{A\,B}\;\overline{C\,D}} = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$$



9. Joint Optimization (3 x 5p = 15p)
The outputs f and g of a two-output circuit are specified with the following expressions:

f (a, b, c, d) = Σm(0, 2, 5, 7, 8, 12, 15) + D(4, 10, 13)
g (a, b, c, d) = Σm(2, 7, 8, 9, 10, 13, 15) + D(0, 6, 14)

(a) Draw the K-map for f and the K-map for g



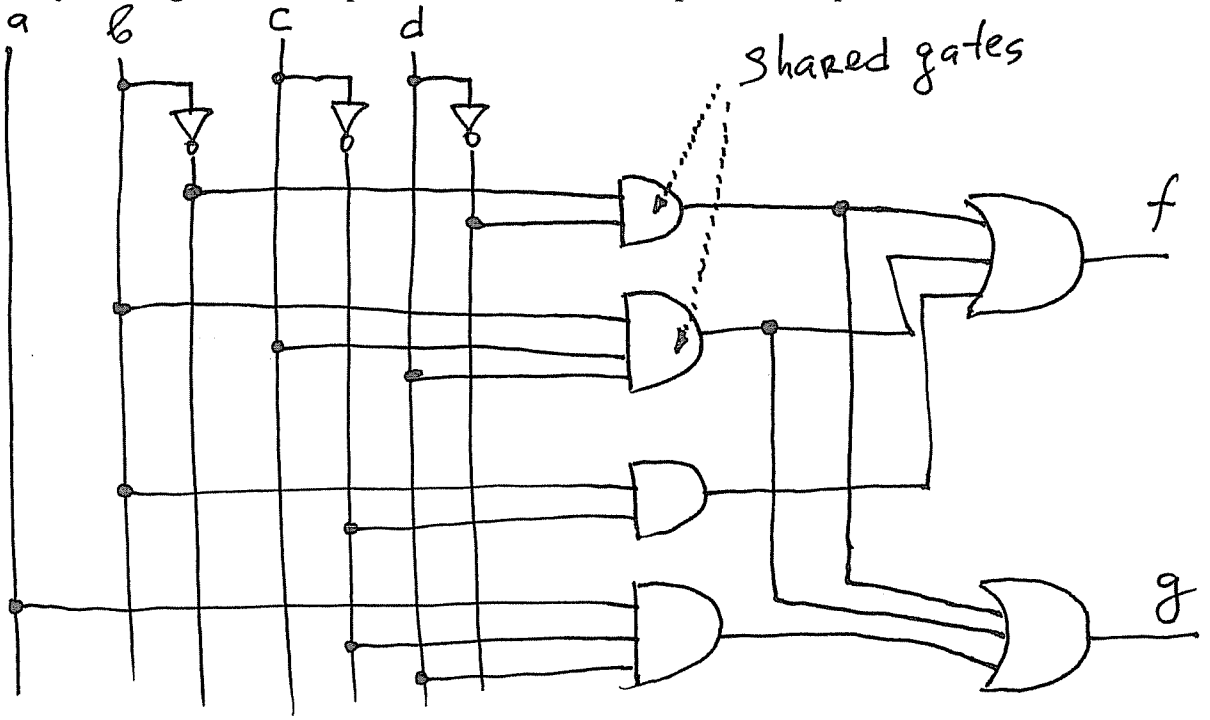
(b) Derive the jointly optimized SOP expressions for f and g such that the two expressions share two implicants. Note that these are not necessarily prime implicants.

$$f = \bar{b}\,\bar{d} + bcd + b\bar{c}$$

$$g = \bar{b}\,\bar{d} + bcd + a\bar{c}d$$

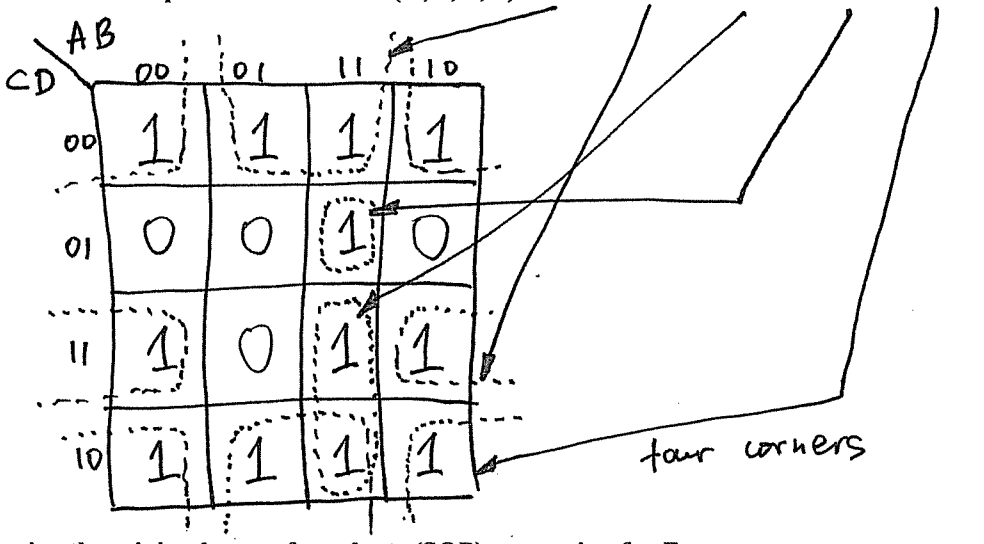
the first two terms are shared

(c) Draw the diagram for the jointly optimized circuit. Indicate which logic gates are shared by drawing arrows that point to them. Label all inputs and outputs.

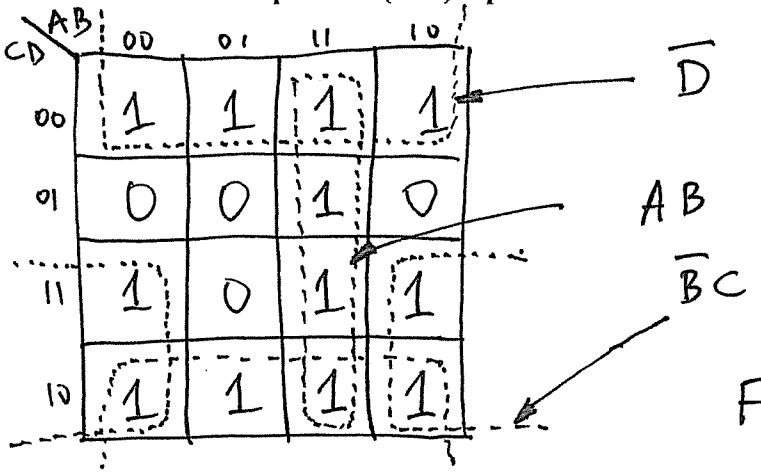


10. More K-maps (3 x 5p = 15p)

(a) Draw the K-map for the function F(A,B,C,D) = $\overline{B}\overline{D} + \overline{B}CD + ABC + AB\overline{C}D + \overline{B}\overline{D}$

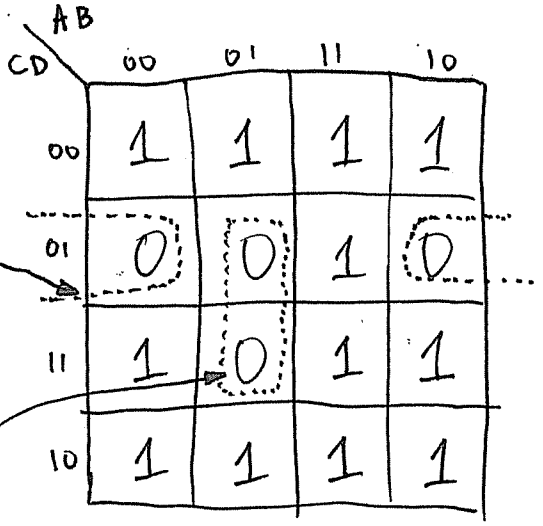


(b) Derive the minimal sum-of-products (SOP) expression for F.



$F = AB + \overline{B}C + \overline{D}$

(c) Redraw the K-map from (a). Derive the minimal product-of-sums (POS) expression for F.



$F = (A+\overline{B}+\overline{D}) \cdot (B+C+\overline{D})$

Question	Max	Score
1. True/False	10	
2. Three-variable K-map	5	
3. Truth Tables	15	
4. Number Conversions	20	
5. Verilog Module	10	
6. Circuit to Circuit	15	
7. SOP with K-Map	15	
8. NAND/NOR Logic	10	
9. Joint Optimization	15	
10. More K-maps	15	
TOTAL:	130	