Cpr E 281 HW 11

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Fourteenth Week
Due Date: Nov. 30, 2015

P1. (15 points) Draw a state transition diagram for:

(a) A state machine that reads in a sequence of binary digits, one at a time, and stops when it has read in a total of five 1s (need not be consecutive). To "stop" the machine, merely have it loop repeatedly in a final state.

(b) A state machine that stops when it has read in at least three consecutive 1s followed by a 0.

P2. (15 points) Design a three-bit counter-like circuit controlled by the input w. If w=0, then the counter subtracts 1 from its contents (acting like a normal down-counter). If w=1, then the counter adds 2 to its contents, wrapping around if the count has to become 8 or 9. Thus if the current state is 6 (or 7) and w=1, then the next state is 0 (or 1). Use D flip-flops in your circuit. Let y_2, y_1, and y_0 be the current state values.

(a) Draw a state diagram for the machine.

(b) Construct a state assignment table including the next state and output.

(c) Write the simplified expressions for the next state and output logic.

P3. (15 points) Repeat problem P2, but now use T flip-flops for your circuit.

P4. (15 points) The arbiter FSM defined in section 6.8 (Figure 6.72) may cause device 3 to never get serviced if devices 1 and 2 continuously keep raising requests, so that in the Idle state it always happens that either device 1 or device 2 has an outstanding request. Modify the proposed FSM to ensure that device 3 will get serviced, such that if it raises a request, the devices 1 and 2 will be serviced only once before the device 3 is granted its request.

P5. (20 points) drive the circuits that implement the state tables shown below. What is the effect of state minimization on the cost of implementation? Please try your best to minimize the cost of your implementations.

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	B	C	1
B	A	F	1
C	F	C	0
F	C	A	0

P6. (20 points) Derive a minimal state table for a single-input and single-output Moore-type FSM that produces an output of 1 if in the input sequence it detects either 110 or 101 patterns. Overlapping sequences should be detected. Repeat this problem for a Mealy-type FSM.