Cpr E 281 HW08

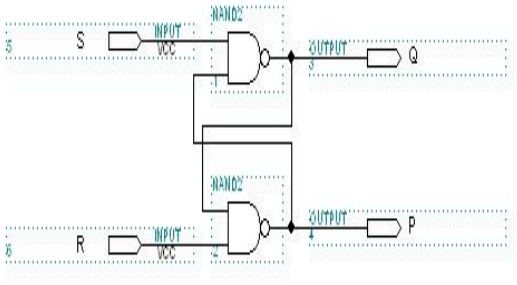
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

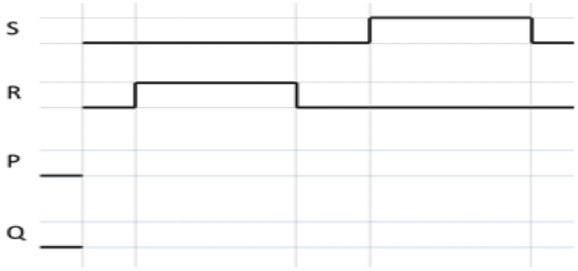
Latches and Flip-Flops
Assigned Date: Ninth Week
Due Date: Oct. 26, 2015

P1. (5 points) Write the truth table for a 1-to-2 decoder. Draw a circuit which implements a 1-to-2 decoder using AND gates, OR gates and NOT gates only.

P2. (20 points) In the circuit below, two NAND gates are used to construct a latch. (Notice that NOR gates are used in the lecture.)

a) For the inputs S and R given below, draw a timing diagram (similar to Fig. 5.4(c) in textbook) for Q and P of the circuit above. You may assume the NAND gates have no delay.

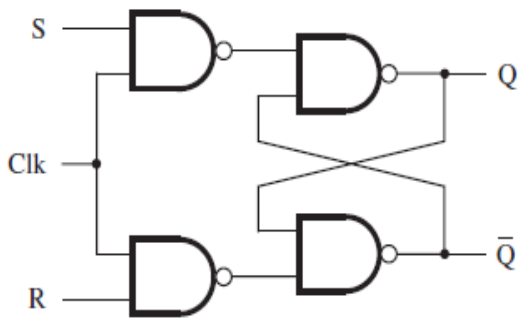


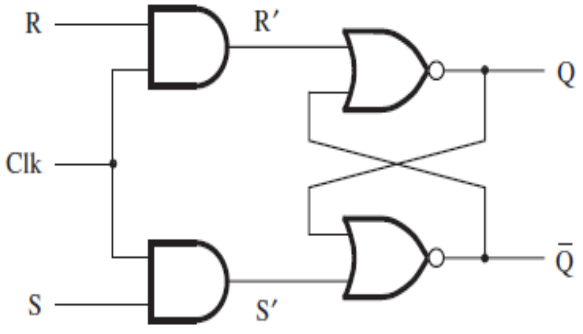


b) Describe what the circuit in P1 above does (i.e., how Q and P are changed) when:

i. R = 0, S = 0;
ii. R = 0, S = 1;
iii. R = 1, S = 0;
iv. R = 1, S = 1;

P3. (10 points) Show that the gated SR latches in the two figures below are functionally equivalent by transforming the first figure to the second using the rules of Boolean algebra. Please show your transformation process step by step using circuit diagrams.





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P4. (30 points) Draw the timing diagram for a negative-edge-triggered D flip-flop with Preset and Clear functionalities for the following input signal combinations. This flip-flop can be seen in Fig. 5.12. The signal values for Clock, D, Preset, and Clear vary as shown below. Assume each signal is held constant from one time step to the next. Assume gate delays to be zero. Assume the initial value of Q to be 0.

a) Draw the waveforms for Clock, D, Preset_n, and Clear_n where Preset_n is the NOT of Preset and Clear_n is the NOT of Clear. Finally, show the output Q.

Time	CLOCK	D	Preset	Clear
0	0	1	0	0
1	1	1	0	0
2	1	1	1	0
3	1	1	0	0
4	1	1	0	1
5	1	1	0	0
6	0	1	0	0
7	0	0	0	1
8	0	0	0	0
9	1	0	0	0
10	0	0	0	0
11	0	1	0	0
12	0	1	1	0
13	0	0	0	0
14	1	0	0	0
15	0	0	0	0

b) Repeat (a) when input D is inverted for all times steps.
c) Repeat (a) for a positive-edge triggered D flip-flop with Preset and Clear. This flip-flop can be seen in Fig. 5.13 in the book.

P5. (20 points) Consider the SR and the JK flip-flops
a) An SR flip-flop has set and reset inputs like a gated SR latch. Show how an SR flip-flop can be constructed using a D flip-flop and other logic gates.
b) Show how a JK flip-flop can be constructed using a T flip-flop and other logic gates.

P6. (15 points) Given a 100-MHz clock signal, derive a circuit using D flip-flops to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming reasonable delays.