Cpr E 281 HW07

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Arithmetic Circuits and Combinational-Circuit Building Blocks
Assigned Date: Eighth Week
Due Date: Oct. 19, 2015

P1. (6 points) Negate the following binary numbers in 4-bit 2's complement representation:
(Remark: Negate means you find the negative of the number.)
(a) 0001
(b) 1100
(c) 0111

P2. (20 points) Consider the addition of the two n-bit 2's complement numbers $X=x_{n-1}\,x_{n-2}\ldots x_1\,x_0$ and $Y=y_{n-1}\,y_{n-2}\ldots y_1\,y_0$. Suppose the sum is $s_{n-1}\,s_{n-2}\ldots s_1\,s_0$ and the carry is $c_n\,c_{n-1}\ldots c_2\,c_1$.
(a) If X is positive, Y is negative, and $c_{n-1}=0$, what should be the values of c_n and s_{n-1} ? Will overflow occur?
(b) If X is negative, Y is negative, and $c_{n-1}=0$, what should be the values of c_n and s_{n-1} ? Will overflow occur?
(c) Following the idea in part (a) and (b), please construct a truth table list the values of c_n and s_{n-1} for all combinations of the sign of X, the sign of Y, and the value of c_{n-1}. For each combination, please also state if overflow occurs or not.
(d) Based on the truth table in part (c), prove that Overflow = $c_n \oplus c_{n-1}$.

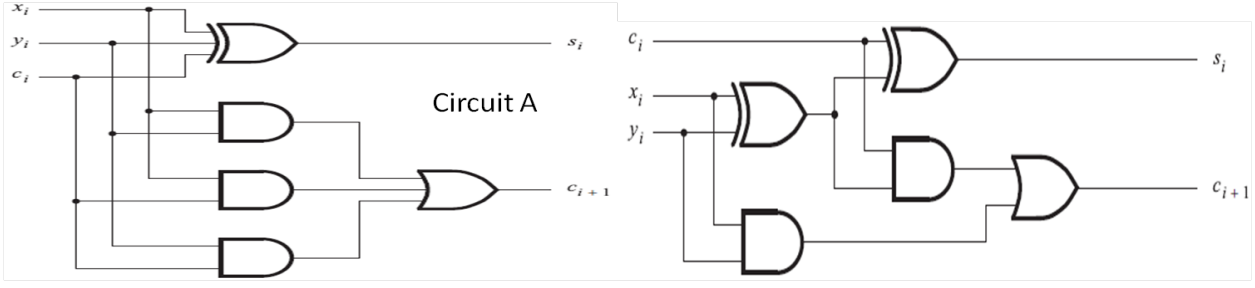
P3. (6 points) Give the 4-bit 2's complement representation for the following decimal numbers:
(a) -6
(b) -1
(c) 6

P4. (10 points) Design a circuit to add 1 to a given n-bit number (i.e., design an increment-by-1 circuit) using n half-adders.

P5. (10 points) Using IEEE 754 SINGLE-PRECISION FLOATING-POINT FORMAT

A) Represent the decimal number 13.5 in IEEE 754 single-precision floating-point format.
B) What is the decimal value of the following IEEE 754 single-precision floating-point number? 10111111 00101000 00000000 00000000

P6. (10 points)Prove that the following two circuits are different representations of the full-adder circuit.



Arithmetic Circuits and Combinational-Circuit Building Blocks
Assigned Date: Eighth Week
Due Date: Oct. 19, 2015

P7. (10 points) Consider constructing a 2^nx1 multiplexer using only 2x1 multiplexers, with n being a positive integer.
(a) How many 2x1 multiplexers would a 2^nx1 multiplexer require? Give an answer in terms of n.
(b) Design an 8x1 multiplexer ($8=2^3$) using a minimal number of 2x1 multiplexers. Please label all signals clearly.

P8. (18 points) Consider a function F with 4 bits of input A_3,A_2,A_1,A_0 such that the output of F is 1 if the unsigned binary number represented by $A_3A_2A_1A_0$ is integer divisible by 3 or 7 (i.e., 0, 3, 6, 7, 9, 12, 14 or 15). Otherwise, the output of F is 0.
(a) Write the truth table for F.
(b) Implement F using a 16x1 MUX and nothing else.
(c) Implement F using an 8x1 MUX, some AND gates, some OR gates, and some NOT gates.

P9. (10 points) Given a supply of 2-to-4 decoders, show how to get a 4-to-16 decoder circuit. Assume each of the 2-to-4 decoders has an ENABLE input (ENABLE = 1 enables the decoder), but you need not include an enable capability on the 4-to-16 decoder circuit.