

DE2 Board I/O Pin Assignments: Switches, LEDs, and 7-Segment Displays

Table 1: Pin assignments for toggle switches

Signal Name	FPGA Pin No.	Description
SW0	PIN_N25	Toggle Switch[0]
SW1	PIN_N26	Toggle Switch[1]
SW2	PIN_P25	Toggle Switch[2]
SW3	PIN_AE14	Toggle Switch[3]
SW4	PIN_AF14	Toggle Switch[4]
SW5	PIN_AD13	Toggle Switch[5]
SW6	PIN_AC13	Toggle Switch[6]
SW7	PIN_C13	Toggle Switch[7]
SW8	PIN_B13	Toggle Switch[8]
SW9	PIN_A13	Toggle Switch[9]
SW10	PIN_N1	Toggle Switch[10]
SW11	PIN_P1	Toggle Switch[11]
SW12	PIN_P2	Toggle Switch[12]
SW13	PIN_T7	Toggle Switch[13]
SW14	PIN_U3	Toggle Switch[14]
SW15	PIN_U4	Toggle Switch[15]
SW16	PIN_V1	Toggle Switch[16]
SW17	PIN_V2	Toggle Switch[17]

Table 2: Pin assignments for pushbutton (debounced) switches

Signal Name	FPGA Pin No.	Description
KEY0	PIN_G26	Pushbutton[0]
KEY1	PIN_N23	Pushbutton[1]
KEY2	PIN_P23	Pushbutton[2]
KEY3	PIN_W26	Pushbutton[3]

Table 3: Pin assignments for LEDs

Signal Name	FPGA Pin No.	Description
LEDR0	PIN_AE23	LED Red[0]
LEDR1	PIN_AF23	LED Red[1]
LEDR2	PIN_AB21	LED Red[2]
LEDR3	PIN_AC22	LED Red[3]
LEDR4	PIN_AD22	LED Red[4]
LEDR5	PIN_AD23	LED Red[5]
LEDR6	PIN_AD21	LED Red[6]
LEDR7	PIN_AC21	LED Red[7]
LEDR8	PIN_AA14	LED Red[8]
LEDR9	PIN_Y13	LED Red[9]
LEDR10	PIN_AA13	LED Red[10]
LEDR11	PIN_AC14	LED Red[11]
LEDR12	PIN_AD15	LED Red[12]
LEDR13	PIN_AE15	LED Red[13]
LEDR14	PIN_AF13	LED Red[14]
LEDR15	PIN_AE13	LED Red[15]
LEDR16	PIN_AE12	LED Red[16]
LEDR17	PIN_AD12	LED Red[17]
LEDG0	PIN_AE22	LED Green[0]
LEDG1	PIN_AF22	LED Green[1]
LEDG2	PIN_W19	LED Green[2]
LEDG3	PIN_V18	LED Green[3]
LEDG4	PIN_U18	LED Green[4]
LEDG5	PIN_U17	LED Green[5]
LEDG6	PIN_AA20	LED Green[6]
LEDG7	PIN_Y18	LED Green[7]
LEDG8	PIN_Y12	LED Green[8]

Using the 7-segment Displays

The DE2 Board has eight 7-segment displays. These displays are arranged as two pairs and a group of four, with the intent of displaying numbers of various sizes. Applying a low logic level to a segment causes it to light up, and applying a high logic level turns it off. Each segment in a display is identified by an index from 0 to 6, with the positions given in Figure 1. Note that the dot in each display is unconnected and cannot be used. Table 4 shows the assignments of FPGA pins to the 7-segment displays.

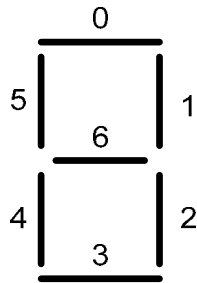


Figure 1: Position and index of each segment in a 7-segment display.

Table 4: Pin assignments for 7-segment displays.

Signal Name	FPGA Pin No.	Description
HEX0 0	PIN_AF10	Seven Segment Digit 0[0]
HEX0 1	PIN_AB12	Seven Segment Digit 0[1]
HEX0 2	PIN_AC12	Seven Segment Digit 0[2]
HEX0 3	PIN_AD11	Seven Segment Digit 0[3]
HEX0 4	PIN_AE11	Seven Segment Digit 0[4]
HEX0 5	PIN_V14	Seven Segment Digit 0[5]
HEX0 6	PIN_V13	Seven Segment Digit 0[6]
HEX1 0	PIN_V20	Seven Segment Digit 1[0]
HEX1 1	PIN_V21	Seven Segment Digit 1[1]
HEX1 2	PIN_W21	Seven Segment Digit 1[2]
HEX1 3	PIN_Y22	Seven Segment Digit 1[3]
HEX1 4	PIN_AA24	Seven Segment Digit 1[4]
HEX1 5	PIN_AA23	Seven Segment Digit 1[5]
HEX1 6	PIN_AB24	Seven Segment Digit 1[6]
HEX2 0	PIN_AB23	Seven Segment Digit 2[0]
HEX2 1	PIN_V22	Seven Segment Digit 2[1]
HEX2 2	PIN_AC25	Seven Segment Digit 2[2]
HEX2 3	PIN_AC26	Seven Segment Digit 2[3]
HEX2 4	PIN_AB26	Seven Segment Digit 2[4]
HEX2 5	PIN_AB25	Seven Segment Digit 2[5]
HEX2 6	PIN_Y24	Seven Segment Digit 2[6]
HEX3 0	PIN_Y23	Seven Segment Digit 3[0]
HEX3 1	PIN_AA25	Seven Segment Digit 3[1]
HEX3 2	PIN_AA26	Seven Segment Digit 3[2]
HEX3 3	PIN_Y26	Seven Segment Digit 3[3]
HEX3 4	PIN_Y25	Seven Segment Digit 3[4]
HEX3 5	PIN_U22	Seven Segment Digit 3[5]
HEX3 6	PIN_W24	Seven Segment Digit 3[6]
HEX4 0	PIN_U9	Seven Segment Digit 4[0]
HEX4 1	PIN_U1	Seven Segment Digit 4[1]
HEX4 2	PIN_U2	Seven Segment Digit 4[2]
HEX4 3	PIN_T4	Seven Segment Digit 4[3]
HEX4 4	PIN_R7	Seven Segment Digit 4[4]
HEX4 5	PIN_R6	Seven Segment Digit 4[5]
HEX4 6	PIN_T3	Seven Segment Digit 4[6]

HEX5 0	PIN_T2	Seven Segment Digit 5[0]
HEX5 1	PIN_P6	Seven Segment Digit 5[1]
HEX5 2	PIN_P7	Seven Segment Digit 5[2]
HEX5 3	PIN_T9	Seven Segment Digit 5[3]
HEX5 4	PIN_R5	Seven Segment Digit 5[4]
HEX5 5	PIN_R4	Seven Segment Digit 5[5]
HEX5 6	PIN_R3	Seven Segment Digit 5[6]
HEX6 0	PIN_R2	Seven Segment Digit 6[0]
HEX6 1	PIN_P4	Seven Segment Digit 6[1]
HEX6 2	PIN_P3	Seven Segment Digit 6[2]
HEX6 3	PIN_M2	Seven Segment Digit 6[3]
HEX6 4	PIN_M3	Seven Segment Digit 6[4]
HEX6 5	PIN_M5	Seven Segment Digit 6[5]
HEX6 6	PIN_M4	Seven Segment Digit 6[6]
HEX7 0	PIN_L3	Seven Segment Digit 7[0]
HEX7 1	PIN_L2	Seven Segment Digit 7[1]
HEX7 2	PIN_L9	Seven Segment Digit 7[2]
HEX7 3	PIN_L6	Seven Segment Digit 7[3]
HEX7 4	PIN_L7	Seven Segment Digit 7[4]
HEX7 5	PIN_P9	Seven Segment Digit 7[5]
HEX7 6	PIN_N9	Seven Segment Digit 7[6]

Table 5: Pin assignments for clock inputs.

Signal Name	FPGA Pin No.	Description
CLOCK_27	PIN_D13	27 MHz clock input
CLOCK_50	PIN_N2	50 MHz clock input
EXT_CLOCK	PIN_P26	External (SMA) clock input