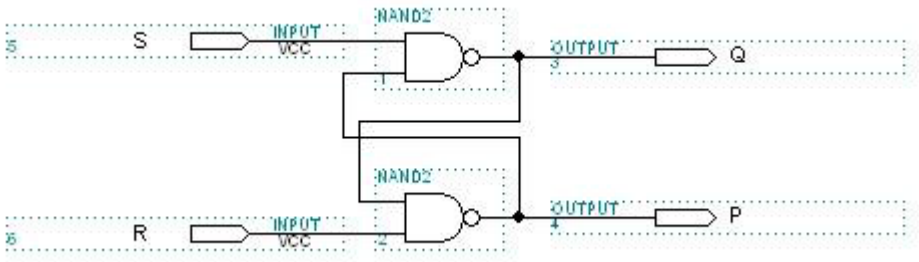
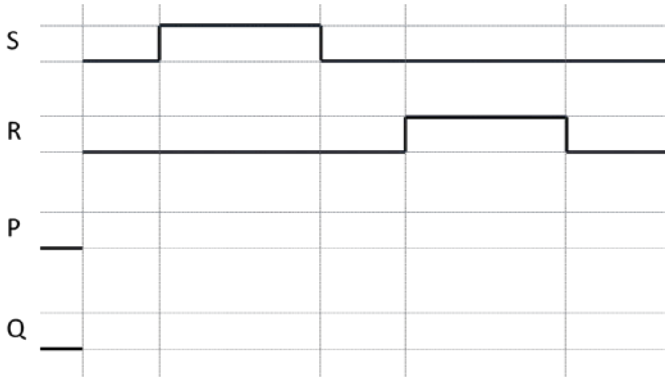
Cpr E 281 HW08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Sequential Circuits
Assigned Date: Ninth Week
Due Date: Mar. 24, 2014

P1. (20 points) In the circuit below, two NAND gates are used to construct a latch. (Notice that NOR gates are used in the lecture.) For the inputs S and R given below, draw a timing diagram (similar to Fig. 5.4(c) in textbook) for Q and P of the circuit above. You may assume the NAND gates have no delay.





P2. (10 points) Describe what the circuit in P1 above does (i.e., how Q and P are changed) when:

(a) R = 0, S = 0;
(b) R = 0, S = 1;
(c) R = 1, S = 0;
(d) R = 1, S = 1;

P3 (10 points) Show that the gated SR latches in Fig. 5.5(a) and Fig. 5.6 are functionally equivalent by transforming the design in Fig. 5.5(a) into the one in Fig. 5.6 using the rules of Boolean algebra. Please show your transformation process step by step using a sequence of circuit diagrams.

P4. (15 points) Explain the behavior of the circuit in Figure 5.12(a) with respect to the following input signal combinations. Assume gate delays to be zero. Assume the initial value of Q to be 0. Draw waveforms for Clock, D, Preset_n, and Clear_n where the signal values for Clock, D, Preset (i.e., NOT of Preset_n), and Clear (i.e., NOT of Clear_n) varies as shown below (assume each time step lasts for a fixed value of time). Show the

output Q. (You do not need to draw any intermediate signals but it is up to you if you like to.)

Time	CLOCK	D	Preset	Clear
0	0	0	0	0
1	0	0	1	0
2	0	0	0	0
3	0	0	0	1
4	0	0	0	0
5	1	0	0	0
6	1	0	1	0
7	1	0	0	0
8	1	0	0	1
9	1	0	0	0
10	0	0	0	0
11	1	0	0	0
12	0	0	0	0
13	0	1	0	0
14	1	1	0	0
15	0	1	0	0

P5. (10 points) Repeat P4 when input D is inverted for all times steps.

P6. (10 points) Repeat P4 for the circuit in Figure 5.13(a). Please note that this flip-flop is positive-edge triggered.

P7. (15 points) Problem 5.1 in the textbook.

P8. (10 points) Problem 5.4 in the textbook.