Cpr E 281 HW07
ELECTRICAL AND COMPUTER
ENGINEERING
IOWA STATE UNIVERSITY

Arithmetic Circuits and
Combinational-Circuit Building Blocks
Assigned Date: Eighth Week
Due Date: Mar. 10, 2014

P1. (10 points) Show that the circuit in Figure 3.4 implements the full-adder specified in Figure 3.3(a).

P2. (15 points) Consider the addition of the two n-bit 2's complement numbers $X=x_{n-1} x_{n-2} \ldots x_1 x_0$ and $Y=y_{n-1} y_{n-2} \ldots y_1 y_0$. Suppose the sum is $s_{n-1} s_{n-2} \ldots s_1 s_0$ and the carry is $c_n c_{n-1} \ldots c_2 c_1$.
(a) If X is positive, Y is negative, and $c_{n-1} =0$, what should be the values of c_n and s_{n-1} ? Will overflow occur?
(b) If X is negative, Y is negative, and $c_{n-1} =0$, what should be the values of c_n and s_{n-1} ? Will overflow occur?
(c) Following the idea in part (a) and (b), please construct a truth table list the values of c_n and s_{n-1} for all combinations of the sign of X, the sign of Y, and the value of c_{n-1}. For each combination, please also state if overflow occurs or not.
(d) Based on the truth table in part (c), prove that Overflow = $c_n \oplus c_{n-1}$.

P3. (10 points) Design a circuit to add 1 to a given n-bit number (i.e., design an increment-by-1 circuit) using n half-adders.

P4. (10 points) Represent the decimal number -7.875 in IEEE 754 single-precision floating-point format.

P5. (10 points) What is the decimal value of the following IEEE 754 single-precision floating-point number?
00111111 01010000 00000000 00000000

P6. (10 points) Design a 8x1 multiplexer using seven 2x1 multiplexers. Please label all signals clearly.

P7. (10 points) The question considers the design of a 8x1 multiplexer using gates. Assume the data inputs are I0,...,I7 and the select inputs are S2, S1 and S0.
(a) Write a sum-of-products expression for the 8x1 multiplexer.
(b) Implement the expression in part (a) using NOT and NAND gates with any number of inputs. Please use as few gates as possible.

P8. (10 points) Consider a function F with 4 bits of input A_3,A_2,A_1,A_0 such that the output of F is 1 if the unsigned binary number represented by $A_3A_2A_1A_0$ is a prime (i.e., 2, 3, 5, 7, 11 or 13). Otherwise, the output of F is 0.
(a) Write the truth table for F.
(b) Implement F using a 16x1 MUX and nothing else.
(c) Implement F using a 8x1 MUX, some AND gates, some OR gates, and some NOT gates.

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P9. (5 points) Write the truth table for a 1-to-2 decoder. Draw a circuit which implements a 1-to-2 decoder using AND gates, OR gates and NOT gates only.

P10. (10 points) Given a supply of 2-to-4 decoders, show how to get a 4-to-16 decoder circuit. Assume each of the 2-to-4 decoders has an ENABLE input (ENABLE = 1 enables the decoder), but you need not include an enable capability on the 4-to-16 decoder circuit.