Sample Solutions

CprE 281: Digital Logic
Midterm 1: Monday Sep 29, 2014

Student Name: **Student ID Number:**

Lab Section: Mon 9-12(N)   Mon 12-3(P)   Mon 5-8(R)   Tue 2-5(M)   Wed 8-11(J)

(circle one)   Thur 2-5(L)   Thur 5-8(K)   Fri 11-2(G)   Fri 5-8(T)

1. **True/False Questions (10 x 1p each = 10p)**

   (a) Chewbacca is an Ewok   TRUE / **FALSE**

   (b) A four input AND gate requires 8 CMOS transistors.   TRUE / **FALSE**

   (c) A two input NOT gate requires 2 CMOS transistors.   TRUE / **FALSE**

   (d) A 4-to-1 multiplexer has only four inputs and one output.   TRUE / **FALSE**

   (e) OR followed by NOT is equivalent to XNOR.   TRUE / **FALSE**

   (f) $a \oplus c = \overline{a} \cdot c + a \cdot \overline{c}$ **TRUE** / FALSE

   (g) It is possible to build a NOT gate with a XNOR gate.   **TRUE** / FALSE

   (h) It is possible to build a NOT gate with a 2-to-1 multiplexer.   **TRUE** / FALSE

   (i) $(a + \overline{b} + c) \cdot (a + \overline{b} + c + d) = (a + \overline{b} + c)$ **TRUE** / FALSE

   (j) I forgot to write down my name and student ID number.   TRUE / **FALSE**

2. **Boolean Expressions (5 x 1p each = 5p)**

Write the value (0 or 1) for each Boolean expression, given the initial conditions.

`A = 1,  B = 0,  C = 1,  D = 0`

   (a) `(AC + DC)`   1

   (b) `(AB + CD)(D + BC)`   0

   (c) `(CC + AA + AB)(AC + BA + BA)`   1

   (d) `(AB + CA)(BC + AC)`   1

   (e) `(A + B + 1)(ABC)`   0

3.Truth Tables (5p + 5p = 10p)
Use a truth table to check if the following Boolean expressions are equivalent.

(a) $(x + y) \cdot \overline{(y \cdot z)} = (y \wedge z) \cdot (x + \bar{x} \cdot y)$

X	Y	Z	Y·Z	$\overline{Y \cdot Z}$	X+Y	LHS	$\bar{X}$	Y∧Z	X+X̄·Y	RHS
0	0	0	0	1	0	0	1	0	0	0
0	0	1	0	1	0	0	1	1	0	0
0	1	0	0	1	1	1	1	1	1	1
0	1	1	1	0	1	0	1	0	1	0
1	0	0	0	1	1	[1]	0	0	1	[0]
1	0	1	0	1	1	1	0	1	1	1
1	1	0	0	1	1	1	0	0	1	1
1	1	1	1	0	1	0	0	0	1	0

They are NOT equal

(b) $x \cdot y \cdot z + (x \wedge y) = x \cdot \overline{(y \cdot \bar{z})} + \bar{x} \cdot y$

X	Y	Z	X·Y·Z	X∧Y	LHS	Y·Z̄	$\overline{Y \cdot \bar{Z}}$	X·(Y·Z̄)	X̄·Y	RHS
0	0	0	0	0	0	0	1	0	0	0
0	0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	1	1	0	0	1	1
0	1	1	0	1	1	0	1	0	1	1
1	0	0	0	1	1	0	1	1	0	1
1	0	1	0	1	1	0	1	1	0	1
1	1	0	0	0	0	1	0	0	0	0
1	1	1	1	0	1	0	1	1	0	1

They are equal

4. Number Conversions (4 x 5p each = 20p)

(a) Convert 132_8 to decimal

$$1 \times 8^2 + 3 \times 8^1 + 2 \times 8^0 = 1 \times 64 + 3 \times 8 + 2 \times 1$$
$$= 64 + 24 + 2$$
$$= 90_{10}$$

(b) Convert 432_{10} to binary

$432 / 2 = 216 \quad 0$
$216 / 2 = 108 \quad 0$
$108 / 2 = 54 \quad 0$
$54 / 2 = 27 \quad 0$
$27 / 2 = 13 \quad 1$
$13 / 2 = 6 \quad 1$
$6 / 2 = 3 \quad 0$
$3 / 2 = 1 \quad 1$
$1 / 2 = 0 \quad 1$

$110110000_2 = 432_{10}$
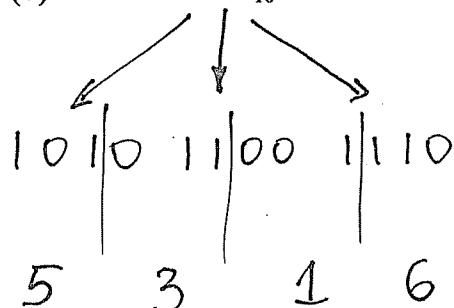
(c) Convert 42_7 to binary:

$$4 \times 7^1 + 2 \times 7^0 = 28 + 2 = 30_{10}$$

$30 / 2 = 15 \quad 0$
$15 / 2 = 7 \quad 1$
$7 / 2 = 3 \quad 1$
$3 / 2 = 1 \quad 1$
$1 / 2 = 0 \quad 1$

$11110_2 = 42_7$
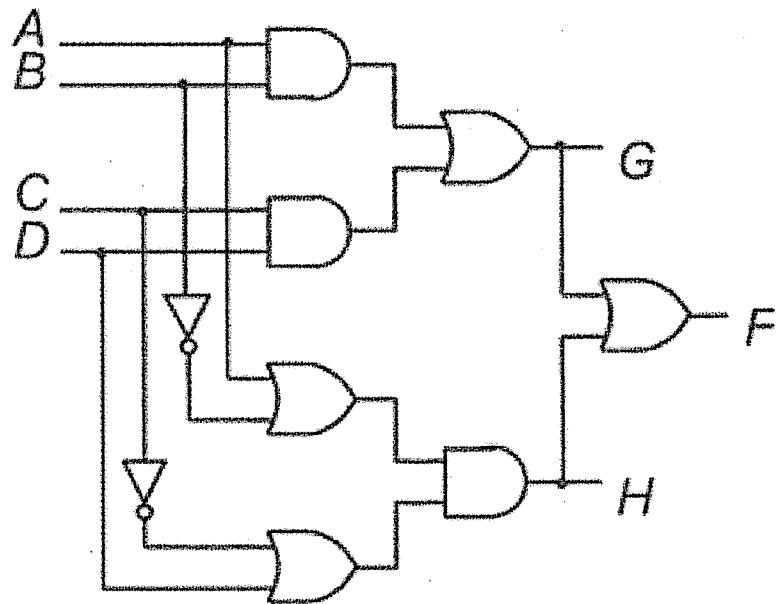
(d) Convert ACE_{16} to octal

$101|0\ 11|00\ 1|110$

$5 \quad 3 \quad 1 \quad 6$

$5316_8 = ACE_{16}$

5. From Logic Circuit to Verilog Code (10p)
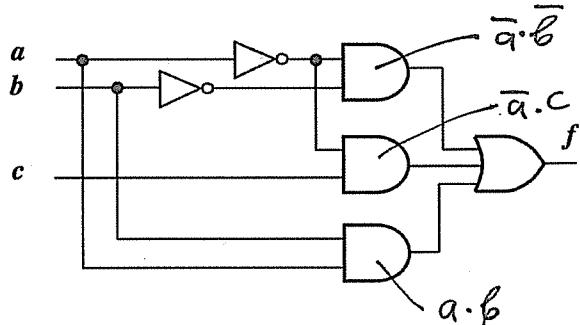
Write a Verilog module for the following logic circuit.


```
module   GFH ( A, B, C, D, G, F, H );
    input   A, B, C, D;
    output  G, F, H;

    assign  G = ( A & B ) | ( C & D );

    assign  H = ( A | ~B ) & ( ~C | D );

    assign  F = G | H;

endmodule
```

**6. Circuit to Circuit Conversion ( 3 x 5p = 15p)**

**(a) Draw the truth table for the function implemented by the following circuit:**



$$\overline{a} \cdot \overline{b}$$

$$\overline{a} \cdot c$$

$$a \cdot b$$
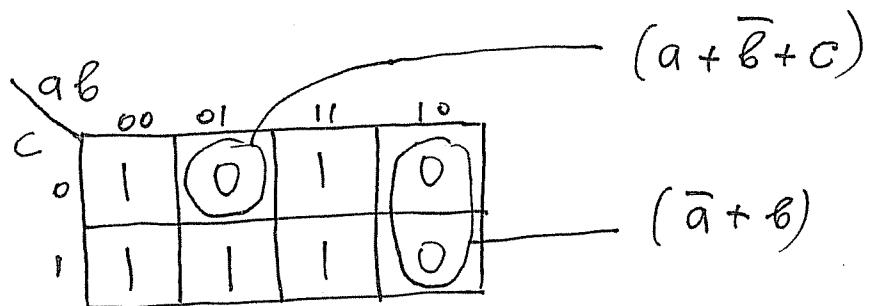
$$f = \overline{a} \cdot \overline{b} + \overline{a} \cdot c + a \cdot b$$

| a b c | $\overline{a}$ | $\overline{b}$ | $\overline{a} \cdot \overline{b}$ | $\overline{a} \cdot c$ | $a b$ | $f$ | |
|-------|-----|-----|------|------|----|----|----|
| 0 0 0 | 1 | 1 | 1 | 0 | 0 | 1 | $m_0$ |
| 0 0 1 | 1 | 1 | 1 | 1 | 0 | 1 | $m_1$ |
| 0 1 0 | 1 | 0 | 0 | 0 | 0 | 0 | $m_2$ |
| 0 1 1 | 1 | 0 | 0 | 1 | 0 | 1 | $m_3$ |
| 1 0 0 | 0 | 1 | 0 | 0 | 0 | 0 | $m_4$ |
| 1 0 1 | 0 | 1 | 0 | 0 | 0 | 0 | $m_5$ |
| 1 1 0 | 0 | 0 | 0 | 0 | 1 | 1 | $m_6$ |
| 1 1 1 | 0 | 0 | 0 | 0 | 1 | 1 | $m_7$ |
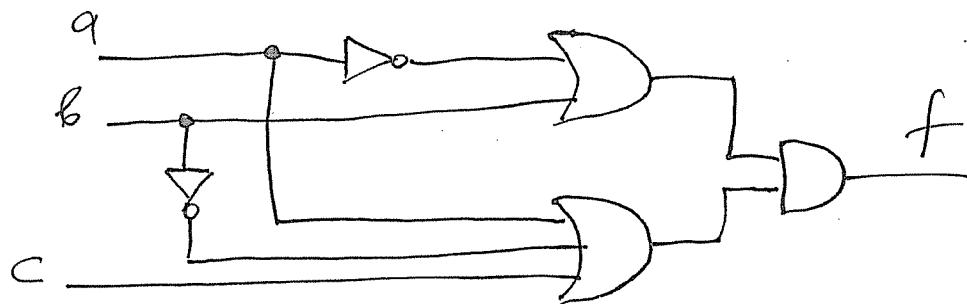
**(b) Use a K-map to derive the minimum-cost Product-of-Sums (POS) expression for f.**



$$(a + \overline{b} + c)$$

$$(\overline{a} + b)$$
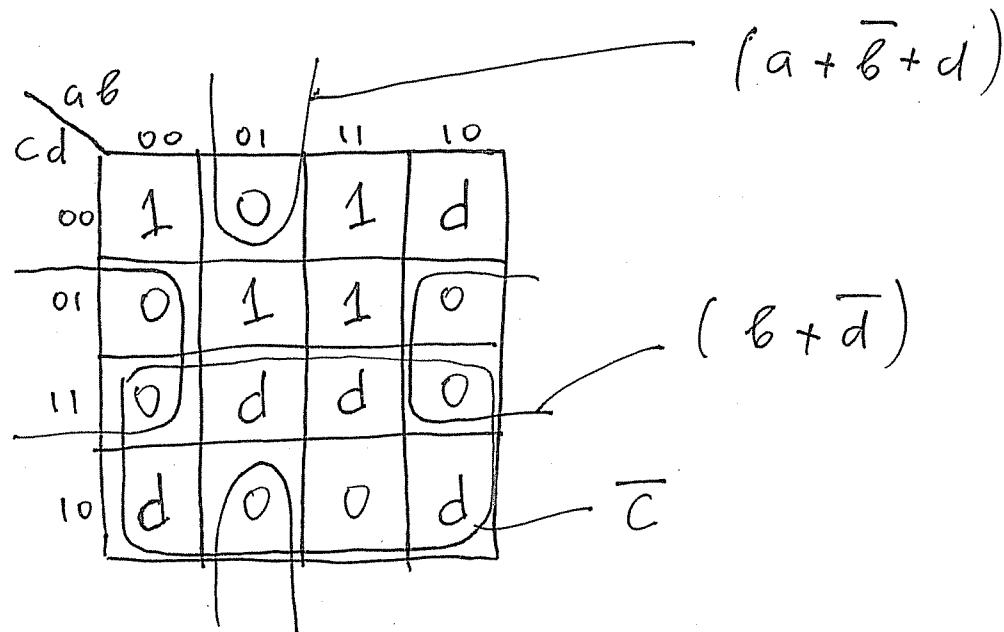
$$f = (\overline{a} + b)(a + \overline{b} + c)$$

**(c) Draw the circuit for the minimum POS expression. Label all inputs and outputs.**
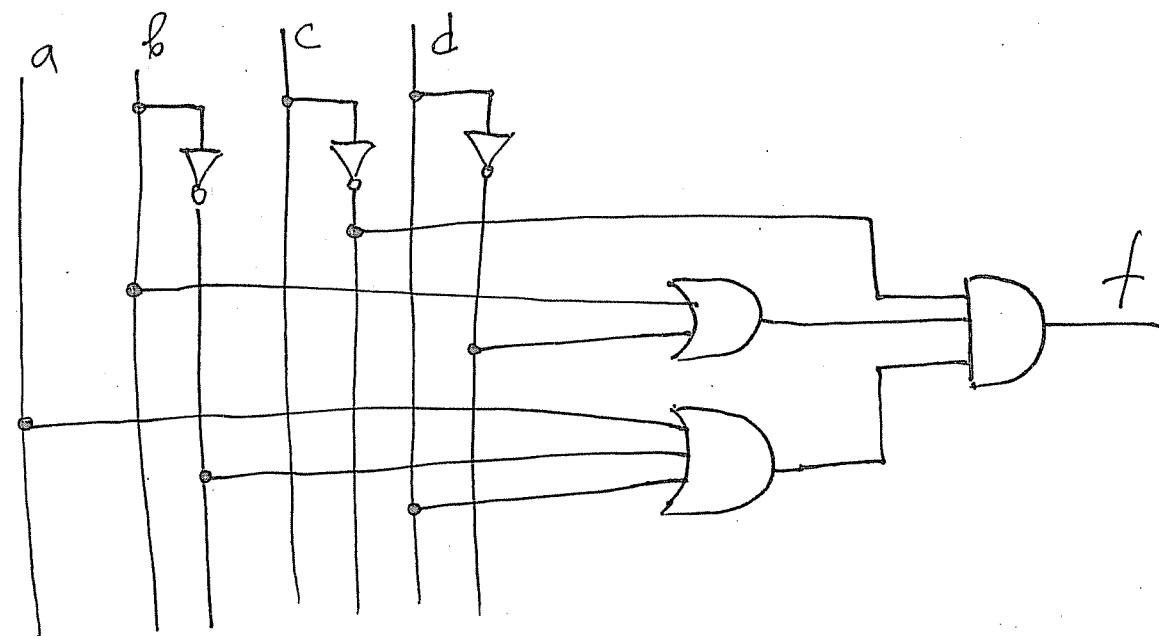
**7. Derive the minimum <u>POS</u> expression using a K-map (10p + 5p = 15p)**

**(a) Use a K-map to derive the minimum-cost <u>POS</u> expression for the following function**

$$f = \Sigma m(0, 5, 12, 13) + D(2, 7, 8, 10, 15)$$

$$(a + \bar{b} + d)$$

| cd \ ab | 00 | 01 | 11 | 10 |
|---------|----|----|----|----|
| 00 | 1 | 0 | 1 | d |
| 01 | 0 | 1 | 1 | 0 |
| 11 | 0 | d | d | 0 |
| 10 | d | 0 | 0 | d |

$$(b + \bar{d})$$

$$\bar{c}$$
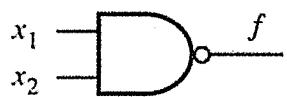
$$f = \bar{c}\,(b + \bar{d})\,(a + \bar{b} + d)$$

**(b) Draw the circuit diagram for the minimum expression.**
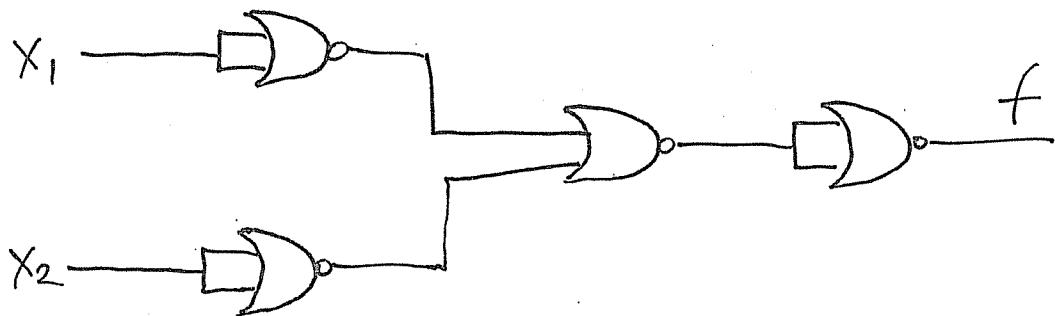
## 8. NAND/NOR Logic (5p + 5p = 10p)
(a) Redraw the following logic circuit using only NOR gates.
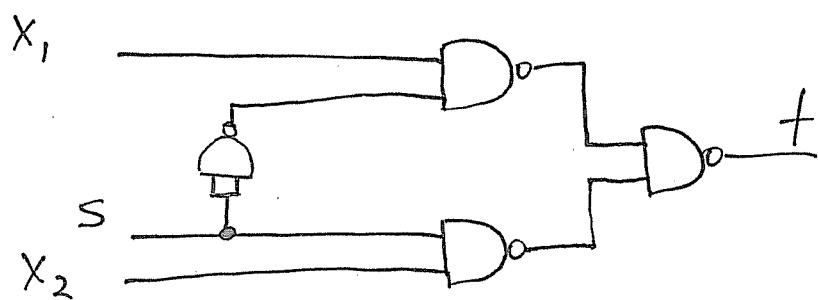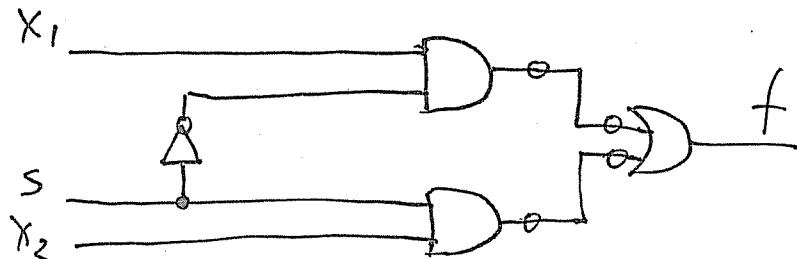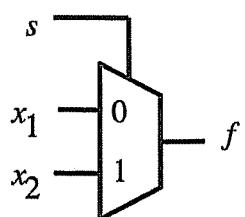


$$\overline{X_1 \cdot X_2} = \overline{\overline{X_1} + \overline{X_2}} = \overline{\overline{\overline{X_1} + \overline{X_2}}}$$



(b) Redraw the following logic circuit using only NAND gates.

**9. Joint Optimization (3 x 5p = 15p)**
The outputs f and g of a two-output circuit are specified with the following expressions:
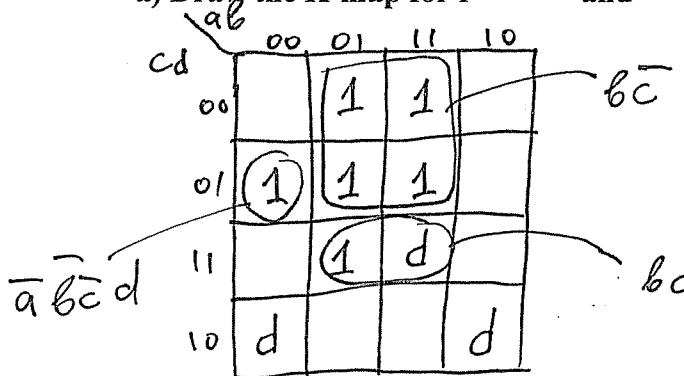
$f(a, b, c, d) = \Sigma m(1, 4, 5, 7, 12, 13) + D(2, 10, 15)$
$g(a, b, c, d) = \Sigma m(1, 4, 6, 14, 15) + D(7, 12)$

**a) Draw the K-map for f       and       the K-map for g**
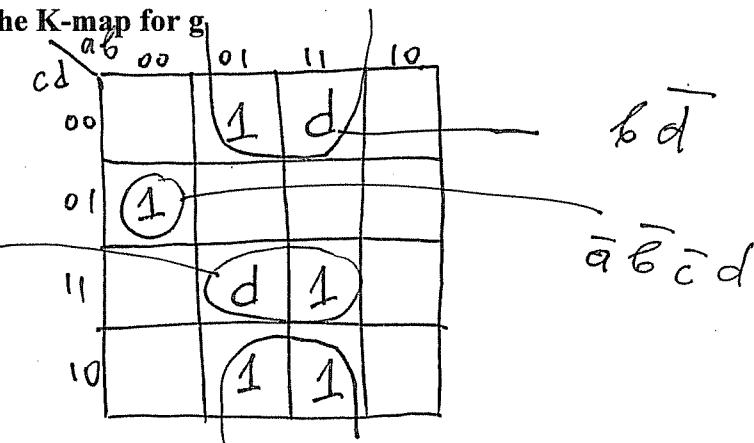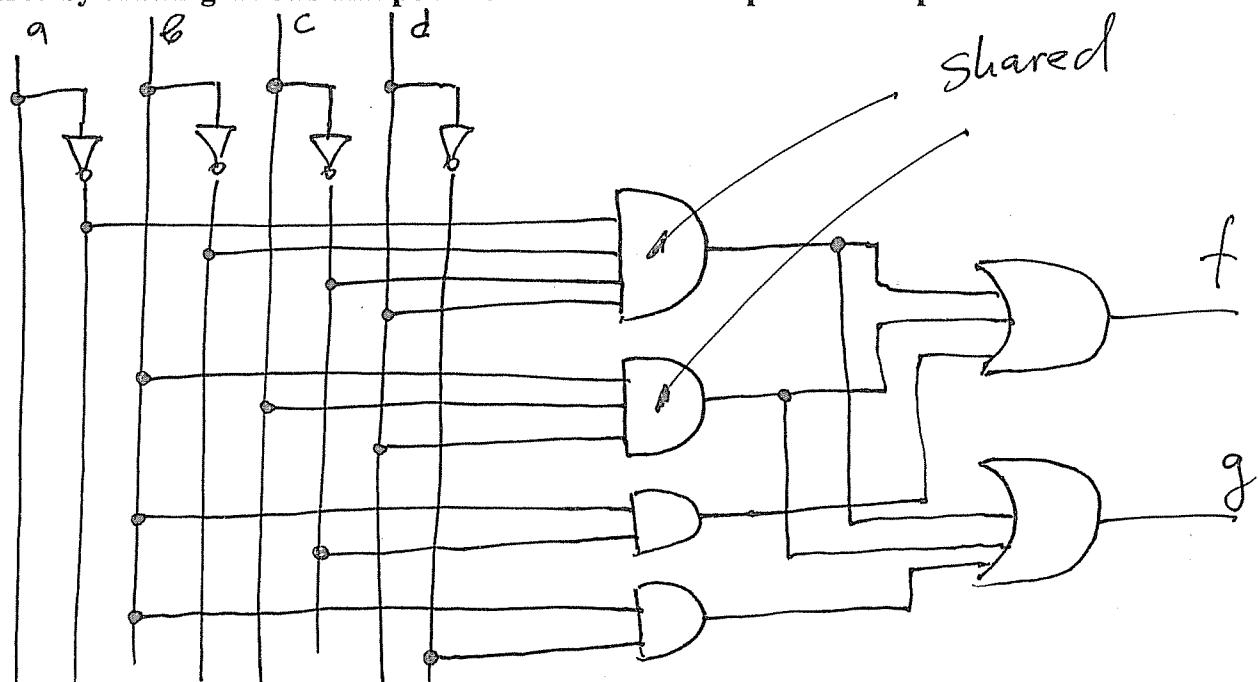


**b) Derive the _jointly optimized SOP_ expressions for f and g such that the two expressions share two implicants. Note that these are not necessarily prime implicants.**

$$f = \overline{a}\,\overline{b}\,\overline{c}\,d + bc d + b\overline{c}$$

$$g = \overline{a}\,\overline{b}\,\overline{c}\,d + bcd + b\overline{d}$$

The first two implicants are shared.

**c) Draw the diagram for the jointly optimized circuit. Indicate which logic gates are shared by drawing arrows that point to them. Label all inputs and outputs.**

**10. Old Manuscript (4 x 5p = 20p)**
You stumble across an old manuscript containing the following page, but some ink stains are obscuring part of the content. Deduce the function F(A,B,C) and write: 1) the complete K-map; 2) the complete truth table; 3) the minimized POS expression; and 4) the minimized SOP circuit diagram.  Explain your reasoning. Use the extra space on the next page if needed.



The manuscript page shows a truth table, a partial POS expression, and a partially obscured SOP circuit:

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

(1) Truth Table

$F(A,B,C) = (A + \bar{B} + C) \cdot$ [obscured]
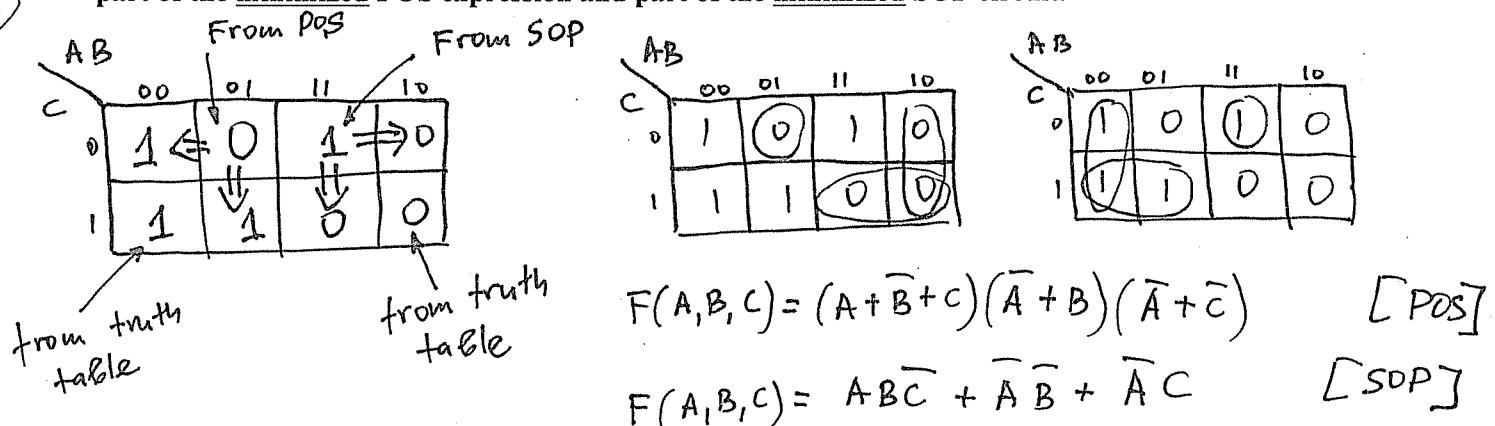
(2) Minimized POS Expression

A   B   C ... $AB\bar{C}$

(3) Minimized SOP Circuit

Representations of function F(A,B,C)

**Hint 1: There is only one unique solution to this problem.**
**Hint 2: You may find it helpful to draw the K-map first and populate it with the information that you are given and then try to infer the rest of its entries. Use the fact that you are given part of the minimized POS expression and part of the minimized SOP circuit.**

① 

From POS → From SOP

| C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |

from truth table          from truth table

| C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |

| C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |

$$F(A,B,C) = (A + \bar{B} + C)(\bar{A} + B)(\bar{A} + \bar{C}) \qquad [POS]$$

$$F(A,B,C) = A B \bar{C} + \bar{A}\bar{B} + \bar{A}C \qquad [SOP]$$
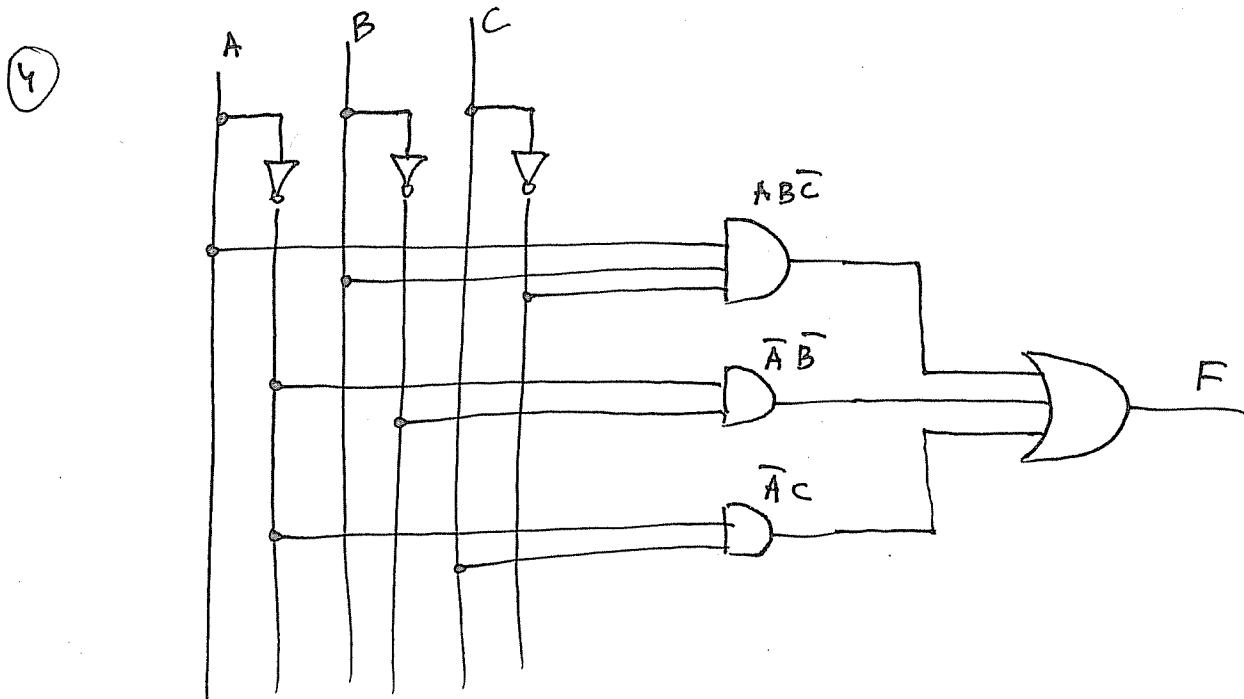
Because we are given the minimized POS expression we know that maxterm $M_2 = (A + \bar{B} + C)$ could not be combined with other maxterms to get a simpler expression. Thus, all adjacent cells to M2 in the K-map cannot be 0; otherwise M2 would not be by itself in the minimized expression. By similar logic, minterm $m_6 = AB\bar{C}$ appears by itself in the minimized SOP circuit. Therefore, it cannot be surrounded by other 1's. Thus, the neighbors of $m_6$ in the K-map must be 0's.

② 

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

③

$$F(A,B,C) = (A + \bar{B} + C)(\bar{A} + B)(\bar{A} + \bar{C})$$

④



| Question | Max | Score |
|---|---|---|
| 1. True/False | 10 | |
| 2. Boolean Expressions | 5 | |
| 3. Truth Tables | 10 | |
| 4. Number Conversions | 20 | |
| 5. Verilog Module | 10 | |
| 6. Circuit to Circuit | 15 | |
| 7. POS with K-Map | 15 | |
| 8. NAND/NOR Logic | 10 | |
| 9. Joint Optimization | 15 | |
| 10. Old Manuscript | 20 | |
| TOTAL: | 130 | |