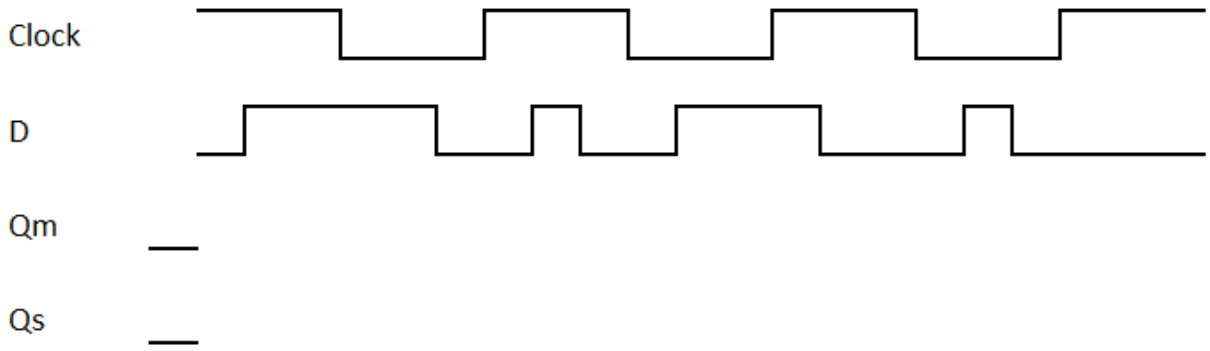
Cpr E 281 HW 09

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Registers and Counters
Assigned Date: Eleventh Week
Due Date: Nov. 10, 2014

P1. (10 points) Consider a positive-edge triggered master-slave D flip-flop design, similar to the negative-edge triggered design in Fig. 9(a) but with the NOT gate in a different location. For the input Clock and D given below, draw a timing diagram of the positive-edge triggered flip-flop for Q_m and Q_s. Then briefly explain why this flip-flip design is positive-edge triggered.



P2. (10 points) Show how a JK flip-flop can be constructed using a T flip-flop and other logic gates.

P3. (10 points) This question considers the construction of a 64-bit register with transistors. Suppose D flip-flops are implemented as shown in Figure 5.9(a) in which gated D latches are implemented as shown in Figure 5.7(a) in textbook. The NAND gates and NOT gates used are implemented as CMOS circuits as discussed in Appendix B. How many transistors are required to implement a 64-bit register?

P4. (20 points) Design a 4-bit register with both shift and parallel load features. The inputs of the register include a 2-bit control code X Y, a 4-bit input value I3 I2 I1 I0, and a clock signal. The outputs of the register are the 4 bits Q3 Q2 Q1 Q0 corresponding to the value stored in the register. You are allowed to use any number of D flip-flops, muxes of any size, decoders and encoders of any sizes, AND gates, OR gates, and NOT gates. (Notice that you do not need all of them.) The operations of the register is defined below:

X Y	Operation
0 0	Hold the current value stored (i.e., Q3 Q2 Q1 Q0 are not changed)
0 1	Shift right (i.e., new Q3=I3, new Q2=Q3, new Q1=Q2, new Q0=Q1)
1 0	Shift left (i.e., new Q3=Q2, new Q2=Q1, new Q1=Q0, new Q0=I0)
1 1	Load new date (i.e., new Q3=I3, new Q2=I2, new Q1=I1, new Q0=I0)

P5. (10 points) To construct a register file containing 8 16-bit registers, two input ports and three output ports, we use **w** 16-bit registers with parallel load input, **x** **y**-to-1 **z**-bit muxes, and **p** **q**-to-**r** decoders with enable. Specify the values of **w**, **x**, **y**, **z**, **p**, **q**, and **r**.

P6. (15 points) Design a 4-bit asynchronous up/down-counter with Enable using T flip-flops and any combinational circuit devices. The direction of the counter is controlled by a 1-bit signal U. If U=1, the counter will count up. If U=0, the counter will count down. The counting can be enabled/disabled by a 1-bit signal E. If E=1, the counter will count whenever there is up-going clock edge. If E=0, the counter will keep the same value stored.

P7. (15 points) Design a 4-bit asynchronous up-counter using JK flip-flops. (Hint: Think of how to implement a T flip-flop using a JK flip-flop.)

P8. (10 points) Bob needs to use a 3-bit up-counter. However, he only has a 4-bit synchronous down-counter and several NOT gates. He is NOT allowed to modify the internal structure of the down-counter. How can he construct the 3-bit up-counter using only the devices he has?