CprE 281: Digital Logic
Midterm 1: Monday Sep 30, 2013

Student Name: **Student ID Number:**

Lab Section: Mon 9-12(N), Tue 2-5(M), Wed 8-11(J), Thu 2-5(L), Thu 5-8(K), Fri 11-2(G) (circle one)

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name and student ID number. TRUE / (FALSE)

(b) A NOT gate can have two but not three inputs. TRUE / (FALSE)

(c) A NAND gate can have four inputs. (TRUE) / FALSE

(d) AND followed by NOT is equivalent to a NAND. (TRUE) / FALSE

(e) NOR followed by NOT is equivalent to XOR. TRUE / (FALSE)

(f) VHDL is the same as Verilog HDL. TRUE / (FALSE)

(g) Minimization with a K-map always produces a unique solution. TRUE / (FALSE)

(h) It is possible to build a NOT gate with a NOR gate. (TRUE) / FALSE

(i) It is possible to build an AND gate with two NOT gates. TRUE / (FALSE)

(j) It is possible to build a NOR gate with 6 CMOS transistors (TRUE) / FALSE

2. Boolean Expressions (5 x 1p each = 5p)

Write the value (0 or 1) for each Boolean expression, given the initial conditions.

```
X = 1
Y = 0
Z = 1
```

(a) (X + Y)Z 1

(b) (ZX + YZ)X 1

(c) (XX + YY + ZZ)(XY + XZ + YZ) 1

(d) (XY + YX)(YZ + ZY) 0

(e) (X + Y + Z)(XYZ) 0

3. **Truth Tables (5p + 10p = 15p)**

Use a truth table to show that the following Boolean expressions are equivalent.

(a) $b \cdot c + a \cdot b + \bar{a} \cdot c = \bar{a} \cdot c + a \cdot b$

a	b	c	bc	ab	$\bar{a}c$	LHS	$\bar{a}c$	ab	RHS
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	1	1	0	1
0	1	0	0	0	0	0	0	0	0
0	1	1	1	0	1	1	1	0	1
1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0
1	1	0	0	1	0	1	0	1	1
1	1	1	1	1	0	1	0	1	1

They are equivalent because LHS = RHS

(b) $(a \cdot b + a \cdot c)(a \cdot b + a \cdot d) = a(b + c \cdot d)$

a	b	c	d	ab	ac	ab	ad	ab+ac	ab+ad	LHS	a	b	cd	b+cd	RHS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0
0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0
0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0
0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	1	0	1	0	1	0	0	0	0
1	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0
1	0	1	1	0	1	0	1	1	1	1	1	0	1	1	1
1	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1
1	1	0	1	1	0	1	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	0	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

They are equivalent because LHS = RHS.

4. Number Conversions (4 x 5p each = 20p)

(a) Convert 123_{15} to decimal

$1 \times 15^2 + 2 \times 15^1 + 3 \times 15^0 =$

$225 + 30 + 3 = 258_{10}$

(b) Convert 312_4 to binary

$11\,01\,10_2$

each digit maps to two bits.

(c) Convert $CAFE_{16}$ to octal

Convert to binary and then to octal.

$1\,|\,100\,|\,101\,|\,011\,|\,111\,|\,110_2$

$1\ 4\ 5\ 3\ 7\ 6_8$

(d) Convert 134_{10} to binary:

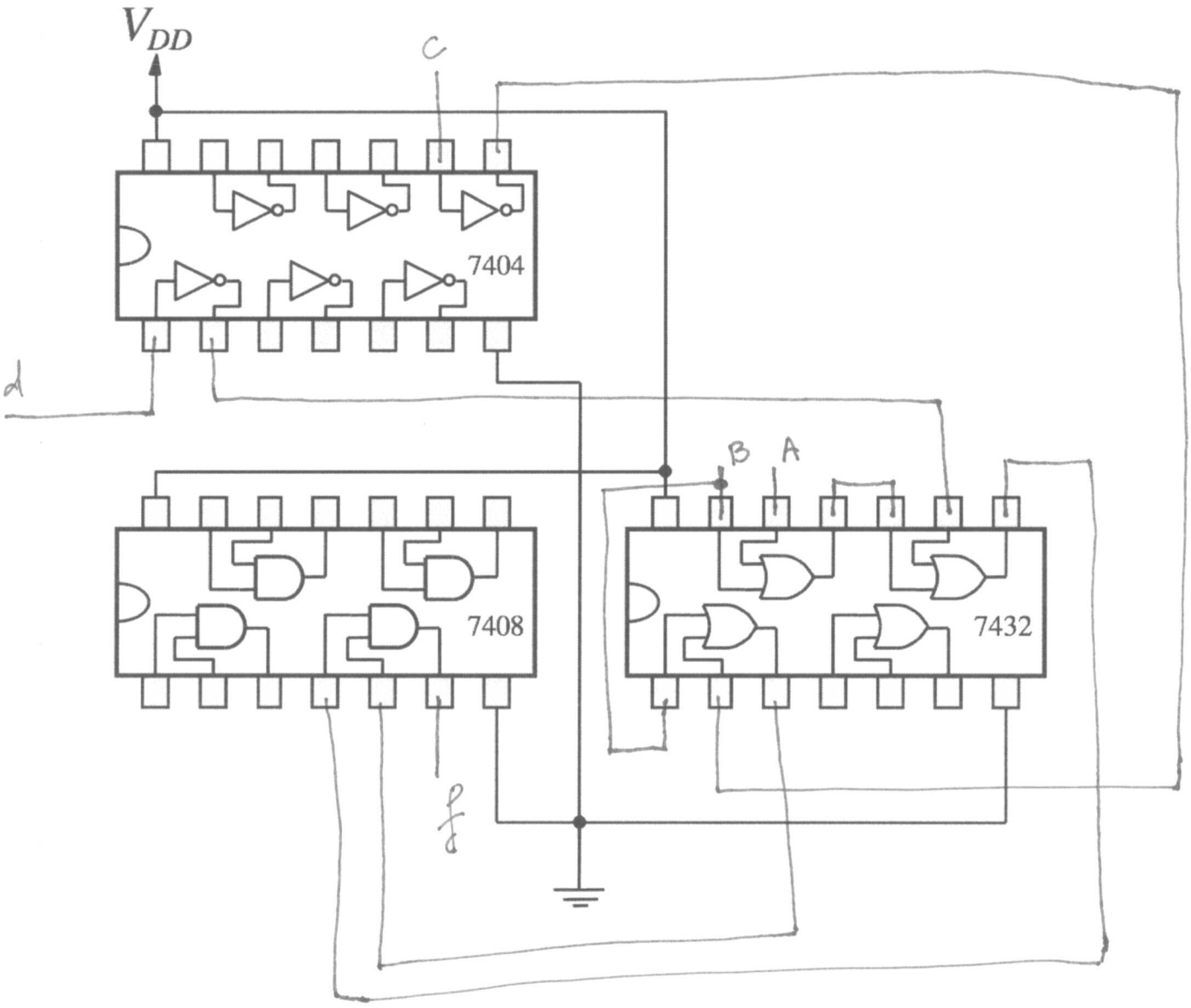
134 / 2 =	67	0
67 / 2 =	33	1
33 / 2 =	16	1
16 / 2 =	8	0
8 / 2 =	4	0
4 / 2 =	2	0
2 / 2 =	1	0
1 / 2 =	0	1

result:

10000110_2

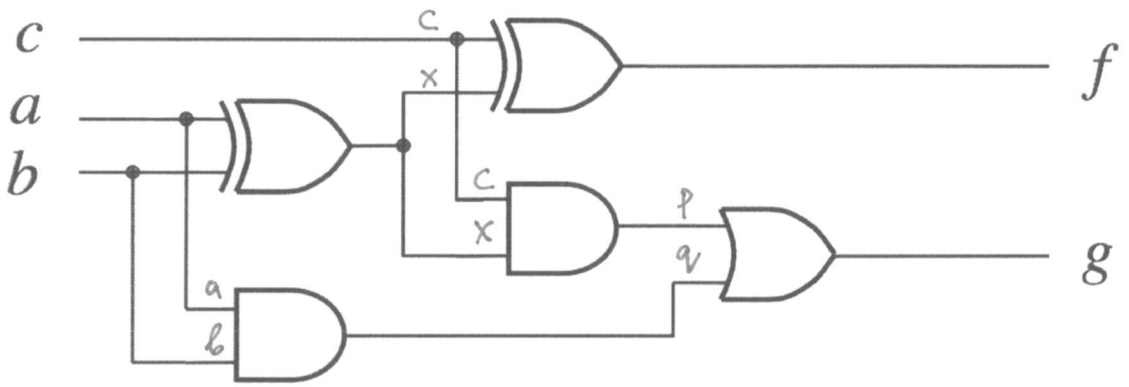
5. **Chip Implementation (10p)**

Implement the Boolean function $f = (a + b + \bar{d})(b + \bar{c})$ using the three chips shown below. Add the necessary wires and labels to get the desired result.



6. From Logic Circuit to Verilog Code (10p)

Write a Verilog module for the following logic circuit.

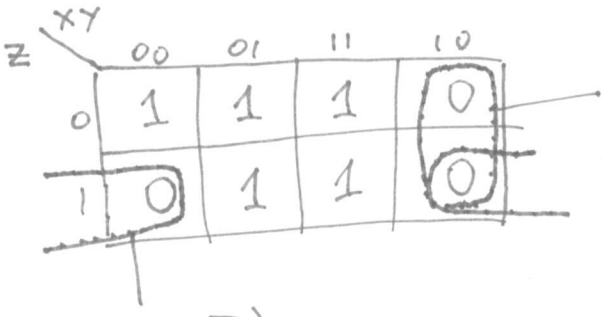



```
module f_g(a, b, c, f, g);
    input a, b, c;
    output f, g;
    wire x, p, q;

    assign x = a ^ b;
    assign p = c & x;
    assign q = a & b;
    assign f = c ^ x;
    assign g = p | q;

endmodule
```

7. Derive the minimum <u>POS</u> expression using a K-map (10p + 5p = 15p)

(a) Use a K-map to derive the minimum-cost POS expression for $f=\overline{x}\,(y+\overline{z}) + x\cdot y$
(b) Draw the circuit diagram for the minimum expression.

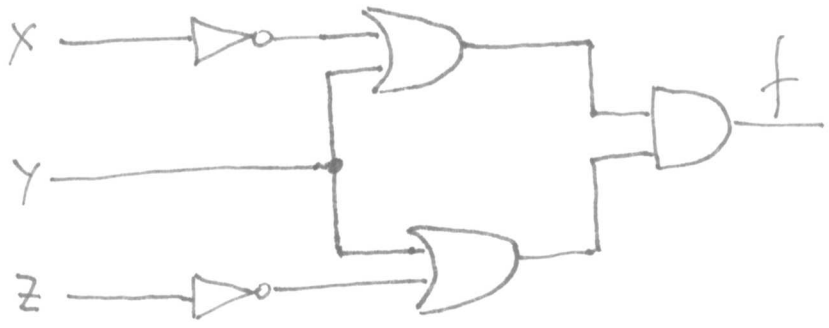
X	Y	Z	$\overline{X}$	$Y+\overline{Z}$	$\overline{X}(Y+\overline{Z})$	XY	f
0	0	0	1	1	1	0	1
0	0	1	1	0	0	0	0
0	1	0	1	1	1	0	1
0	1	1	1	1	1	0	1
1	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	1	0	1	1
1	1	1	0	1	0	1	1



$(\overline{X}+Y)$

$(Y+\overline{Z})$

$f = (\overline{X}+Y)(Y+\overline{Z})$

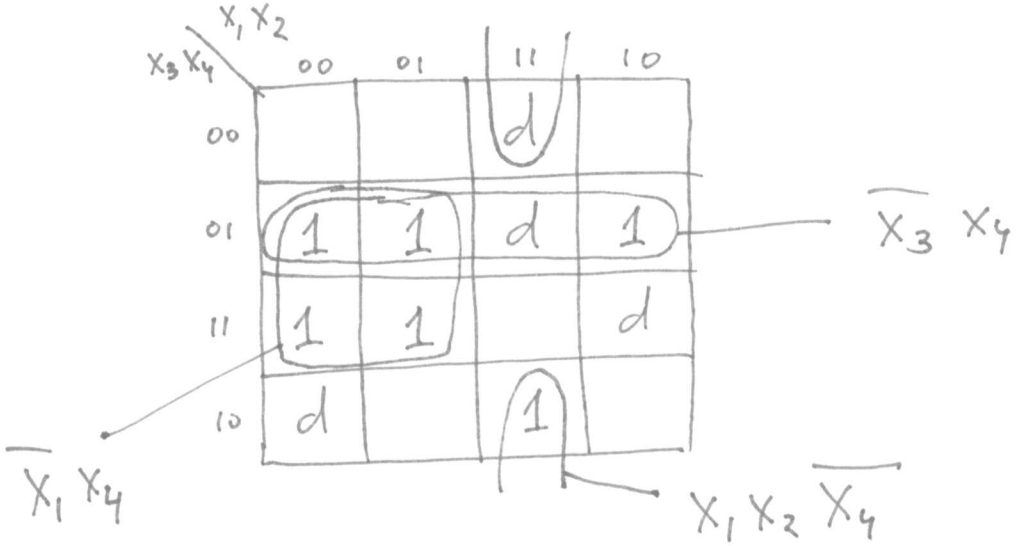


8. Derive the minimum SOP expression using a K-map (10p + 5p = 15p)

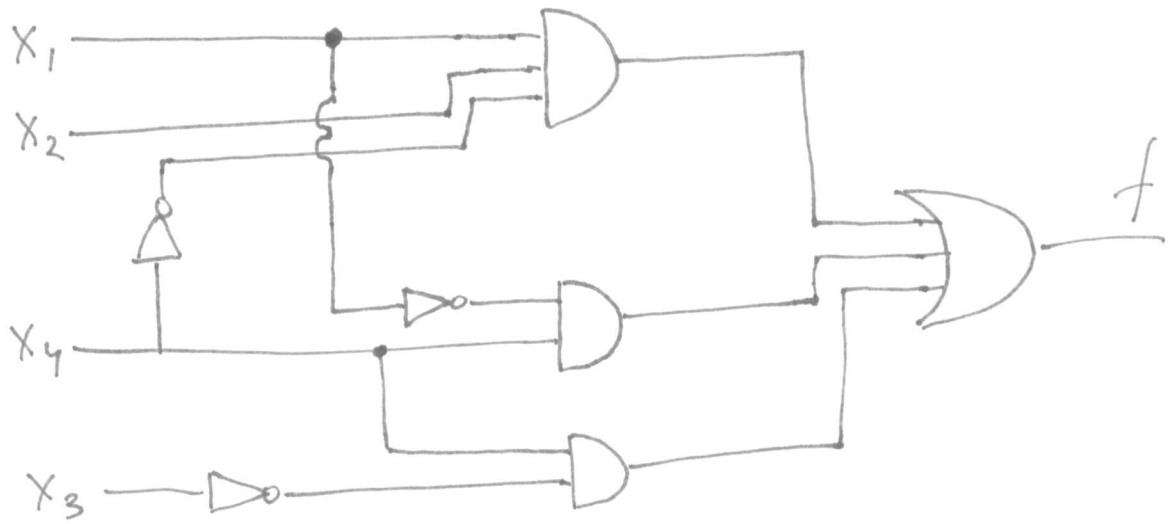
(a) Use a K-map to derive the minimum-cost SOP expression for the following function

$f=\Sigma m(1,3,5,7,9,14) + D(2, 11, 12, 13)$

(b) Draw the circuit diagram the minimum expression.

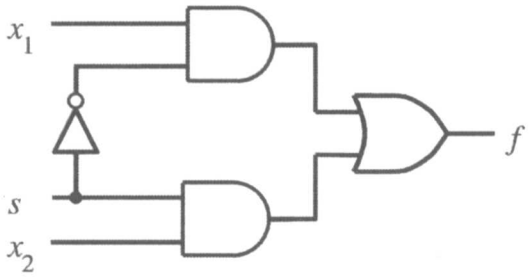


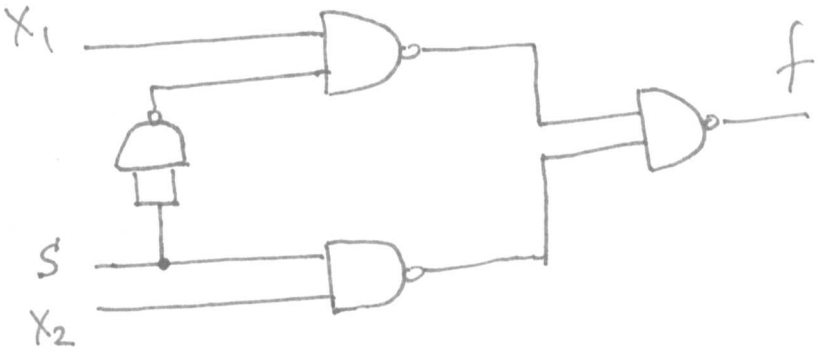
$$f = \overline{X_1}\,X_4 + \overline{X_3}\,X_4 + X_1 X_2 \overline{X_4}$$



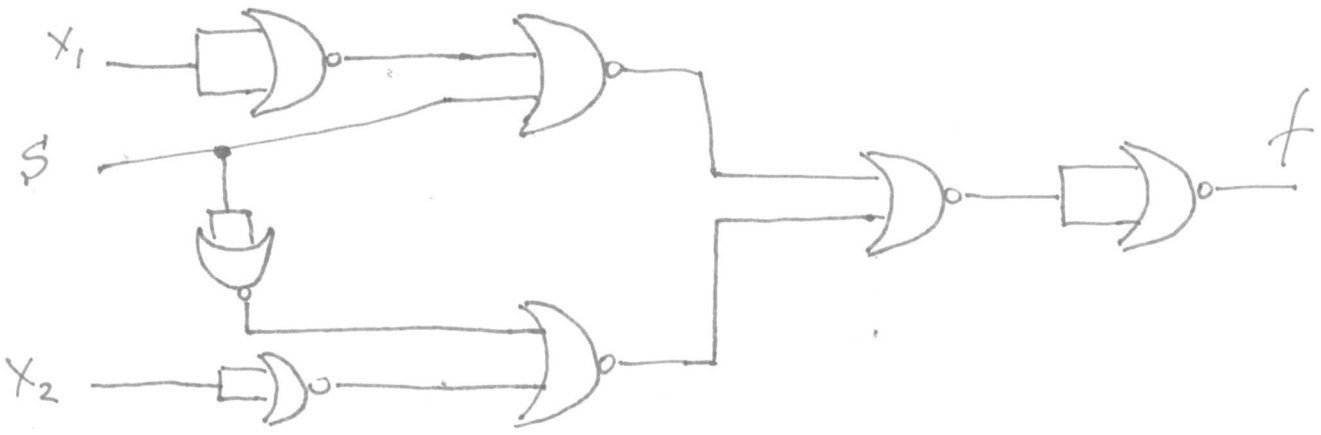
9. NAND/NOR Logic (5p + 10p = 15p)

(a) Redraw the following logic circuit using only NAND gates.





(b) Redraw the original logic circuit from (a) using only NOR gates.



10. Boolean Logic (15p)
Use the theorems of Boolean algebra to simplify the following expression:

$$\bar{x}_1\bar{x}_2x_3 + \bar{x}_1x_2\bar{x}_3 + \bar{x}_1x_2x_3 + x_1\bar{x}_2\bar{x}_3 + x_1\bar{x}_2x_3 + x_1x_2\bar{x}_3 + x_1x_2x_3$$

$$\bar{X}_1(\underbrace{\bar{X}_2 + X_2}_{1})X_3 + (\underbrace{\bar{X}_1 + X_1}_{1})X_2\bar{X}_3 + X_1\bar{X}_2(\underbrace{\bar{X}_3 + X_3}_{1}) + X_1X_2X_3 =$$

$$\bar{X}_1X_3 + X_2\bar{X}_3 + X_1\bar{X}_2 + X_1X_2X_3 =$$

$$\bar{X}_1X_3 + X_2\bar{X}_3 + X_1(\underbrace{\bar{X}_2 + X_2X_3}_{\bar{X}_2 + X_3}) =$$

$$\bar{X}_1X_3 + X_2\bar{X}_3 + X_1\bar{X}_2 + X_1X_3 =$$

$$(\underbrace{\bar{X}_1 + X_1}_{1})X_3 + X_2\bar{X}_3 + X_1\bar{X}_2 =$$

$$\underbrace{X_3 + X_2\bar{X}_3}_{X_3 + X_2} + X_1\bar{X}_2 =$$

$$X_3 + \underbrace{X_2 + X_1\bar{X}_2}_{X_2 + X_1} =$$

$$X_3 + X_2 + X_1$$

Question	Max	Score
1. True/False	10	
2. Expressions	5	
3. Truth Tables	15	
4. Number Conversions	20	
5. Chip Implementation	10	
6. Verilog Module	10	
7. POS with K-Map	15	
8. SOP with K-Map	15	
9. NAND/NOR Logic	15	
10. Boolean Logic	15	
TOTAL:	130	