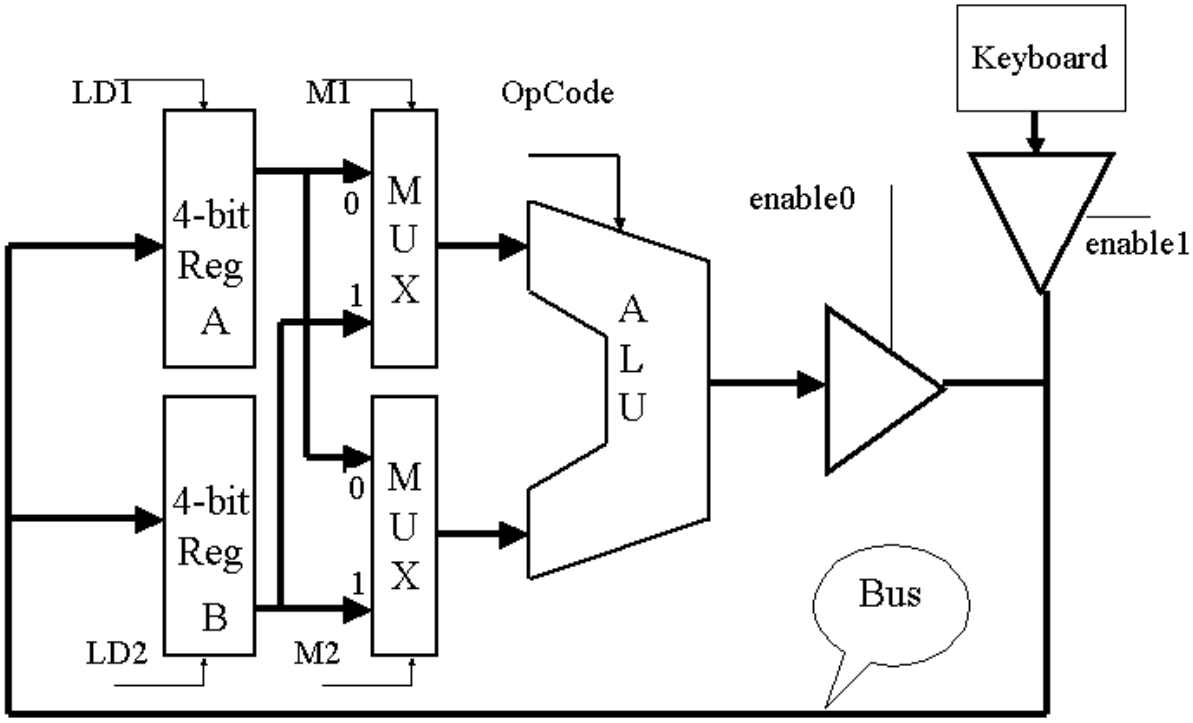
Cpr E 281 HW 11
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Arithmetic Circuits
Assigned Date: Fourteenth Week
Due Date: Dec. 9, 2013

P1. (10 points) Design an n-bit 8-to-1 multiplexer using one 3-to-8 decoder and eight n-bit tri-state buffers.

P2. (30 points) Consider the circuit below. Answer the following questions.



Describe what will happen when the clock arrives if the control signals are as follows for each case. Assume that the ALU block performs the following operations based on the OpCode input: 00 (ADD); 01 (SUB); 10 (AND) and 11 (OR)

Signals	LD1	LD2	M1	M2	OpCode	enable0	enable1
Case 1	1	0	0	1	00	0	1
Case 2	0	1	1	0	00	0	1
Case 3	1	0	0	1	00	1	0
Case 4	1	0	0	1	10	1	0
Case 5	0	1	1	0	01	1	0
Case 6	0	1	1	0	01	1	0

P3. (10 points) Give the clock period corresponding to the following clock frequencies:
(i) 25 Hz; (ii) 2.5 MHz.

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P4. (30 points) For a state machine, suppose that the propagation and contamination delays of the next state circuit are 20 nsec and 5 nsec, respectively. For the registers to store the current state, the propagation delay, set-up time, and hold time are 4 nsec, 2 nsec, and 2 nsec, respectively. Show work in each of the cases below.

(a) What is the minimum clock period required for this state machine?

(b) When can the external inputs be changed after a rising clock edge for proper operation?

(c) For how long should the external inputs be held stable for proper operation? (Consider the total time needed before and after a rising clock edge.)

P5. (20 points) You want to compare two n-bit signed numbers, A and B, and generate A>B, A=B, and A<B signal. Design a one-bit block that can be cascaded together to generate the final signal. Assume that you are allowed to generate a different block to treat the signed bit. Show the design for the two blocks and the complete circuit.