Cpr E 281 HW 09
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Arithmetic Circuits
Assigned Date: Twelfth Week
Due Date: Nov. 18, 2013

P1. (10 points) Problem 5.25 in the book.

P2. (20 points) A full adder takes two input bits and a carry-in bit from a previous stage and produces a sum bit and a carry-out bit as its two outputs. It produces these two outputs in 20 nsec. 1 nsec = 10^{-9} second. One bit full adders can be cascaded by attaching the carry-out of one adder to the carry-in of the next adder in sequence to build an n-bit ripple-carry adder (see Fig. 3.5 in textbook for reference).
(a) Give a formula in terms of n to produce the n-bit sum and carry-out outputs.
(b) Suppose, it takes 15 nsec to produce the carry-out output and 25 nsec to produce the sum output for 1-bit adder. How long does it take to produce the n-bit sum outputs?

P3. (15 points) Consider the D flip-flop shown in Figure 5.9a in the textbook. Suppose the gate delay for NAND gates and NOT gates are 3 nsec and 2 n-sec, respectively.
(a) What is the hold time for the D flip-flop?
(b) What is the set-up time for the D flip-flop?
(c) What is the propagation delay for the D flip-flop?

P4. (20 points) Design a 4-bit register with both shift and parallel load features. The inputs of the register include a 2-bit control code X Y, a 4-bit input value I3 I2 I1 I0, and a clock signal. The outputs of the register are the 4 bits Q3 Q2 Q1 Q0 corresponding to the value stored in the register. You are allowed to use any number of D flip-flops, muxes of any size, decoders and encoders of any number of AND, OR, and NOT gates. (Notice that you do not need all of them.) The operations of the register is defined below:

X Y Operation
0 0 Hold the current value stored (i.e., Q3 Q2 Q1 Q0 are not changed)
0 1 Shift right (i.e., new Q3=I3, new Q2=Q3, new Q1=Q2, new Q0=Q1)
1 0 Shift left (i.e., new Q3=Q2, new Q2=Q1, new Q1=Q0, new Q0=I0)
1 1 Load new date (i.e., new Q3=I3, new Q2=I2, new Q1=I1, new Q0=I0)

P5. (10 points) To construct a register file containing 16 8-bit registers, one input port and three output ports, we use **w** 8-bit registers with parallel load input, **x** **y**-to-1 **z**-bit muxes, and **p** **q**-to-**r** decoder with enable. Specify the values of **w**, **x**, **y**, **z**, **p**, **q**, and **r**.

P6. (15 points) Design a 4-bit asynchronous up-counter using JK flip-flops. (Hint: Think of how to implement a T flip-flop using a JK flip-flop.)

P7. (10 points) Bob needs to use a 3-bit down-counter. He bought one 4-bit synchronous up-counter, which outputs both Q and Q' for each bit. How can he construct the 3-bit down-counter using only the devices he has?