

Curriculum Vitae
JOSEPH ZAMBRENO

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APPOINTMENTS

2006–present Assistant Professor of Electrical and Computer Engineering, Iowa State University
2001–2006 Graduate Research Assistant, Northwestern University

PROFESSIONAL PREPARATION

Northwestern University	Evanston, IL	Electrical and Computer Engineering	Ph.D.	2006
Northwestern University	Evanston, IL	Electrical and Computer Engineering	M.S.	2002
Northwestern University	Evanston, IL	Computer Engineering	B.S.	2001

RESEARCH INTERESTS

- Computer architecture and compilers
- Reconfigurable computing and FPGAs
- Computer security, cryptography, and software protection
- Embedded systems and high-level design methodologies
- Low-power and power-aware computing

HONORS AND AWARDS

May 2011 Warren B. Boast Undergraduate Teaching Award, Iowa State University
May 2009 Warren B. Boast Undergraduate Teaching Award, Iowa State University
June 2006 EECS Department Best Dissertation Award, Northwestern University
2005–2006 Northwestern University Graduate Research Fellowship
2002–2005 National Science Foundation Graduate Research Fellowship
2001–2002 Walter P. Murphy Fellowship
June 2001 Graduation with distinction *summa cum laude*, Northwestern University
2000–2001 Motorola Undergraduate Research Award
2000–present Tau Beta Pi Engineering Honors Society
2000–present Eta Kappa Nu Electrical and Computer Engineering Honors Society

TEACHING EXPERIENCE

1. CprE 480X - *Graphics Processing and Architecture*, Iowa State University. Semesters taught: S11.
2. CprE 185 - *Introduction to Computer Engineering and Problem Solving I*, Iowa State University. Semesters taught: S10.

3. CprE 594 - *Embedded Systems Research Skills*, Iowa State University. Semesters taught: S09 (with P. Jones).
4. CprE 381 - *Computer Organization and Assembly Level Programming*, Iowa State University. Semesters taught: F08, F09, F10.
5. CprE 588 - *Embedded Computer Systems*, Iowa State University. Semesters taught: S07 (with D. Rover), S08, S09, S10.
6. CprE 583 - *Reconfigurable Computing*, Iowa State University. Semesters taught: F06, F07.
7. ECE 510 - *Computer Security and Information Assurance*, Northwestern University. Quarters taught: S05 (with A. Choudhary), S04 (with A. Choudhary).
8. ECE 362 - *Computer Architecture Projects*, Northwestern University. Quarters taught: W05 (with A. Choudhary), W04 (with A. Choudhary).

PROFESSIONAL ACTIVITY

Technical and Organizing Committees

- Technical Program Committee, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2011
- Technical Program Committee, International Conference on High Performance Computing (HiPC), Student Research Symposium, 2009–2011
- Technical Program Committee, IEEE International Conference on Microelectronic Systems Education (MSE), 2009
- SIGDA University Booth Organizer, Design Automation Conference (DAC), 2008–2011
- Publicity Chair + Technical Program Committee, IEEE International Conference on Electro/Information Technology (EIT), 2008
- Student Advocate, International Symposium on Microarchitecture (MICRO), 2007
- Technical Program Committee, International Workshop on High Performance Data Mining (HPDM), 2007

Reviewing Activities

- ACM Transactions on Embedded Computing Systems (TECS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Transactions on Reconfigurable Technology and Systems (TRETTS)
- IEEE/ACM Transactions on Networking (TNET)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Circuits and Systems I (TCAS-I)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computer Aided Design (TCAD)
- IEEE Transactions on Dependable and Secure Computing (TDSC)
- IEEE Transactions on Parallel and Distributed Systems (TPDS)
- IEEE Transactions on Information Forensics and Security (TIFS)
- IEEE Computer

- IEEE Micro
- EURASIP Journal on Advances in Signal Processing
- IEE Proceedings on Information Security
- International Journal of Computers and Applications (IJCA)
- International Journal of Computers and Electrical Engineering
- Journal of Systems and Software (JSS)
- The Journal of Supercomputing (TJS)
- Journal of Microprocessors and Microsystems
- International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
- International Symposium on Microarchitecture (MICRO)
- International Symposium on High-Performance Computer Architecture (HPCA)
- International Conference for High Performance Computing, Networking, Storage, and Analysis (SC)
- Design Automation Conference (DAC)
- International Conference on VLSI Design (VLSID)
- International Conference on Computer Design (ICCD)
- Asia and South Pacific Design Automation Conference (ASP-DAC)
- IEEE International Symposium on Network Computing and Applications (NCA)
- International Symposium on Information Processing in Sensor Networks (IPSN)

Professional Memberships

- IEEE (2002–present)
- IEEE Computer Society (2004–present)
- ACM (2011–present)
- ACM SIGDA (2011–present)

PUBLICATIONS

Journal Papers

1. S. Sun, M. Monga, P. Jones, and **J. Zambreno**. “An I/O Bandwidth-Sensitive Sparse Matrix-Vector Multiplication Engine on FPGAs”, *IEEE Transactions on Circuits and Systems I (TCAS-I)*, 2011. (to appear)
2. A. Pande and **J. Zambreno**. “Poly-DWT: Polymorphic Wavelet Hardware Support For Dynamic Image Compression”, *ACM Transactions on Embedded Computing Systems (TECS)*, 2011. (to appear)
3. A. Pande and **J. Zambreno**. “A Chaotic Encryption Scheme for Real-time Embedded Systems: Design and Implementation”, *Telecommunication Systems*, 2011. (to appear)
4. S. Sun and **J. Zambreno**. “Design and Analysis of a Reconfigurable Platform for Frequent Pattern Mining”, *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 22, no. 9, pp. 1497-1505, 2011.

5. A. Pande and **J. Zambreno**. “Efficient Mapping and Acceleration of AES on Custom Multi-Core Architectures”, *Concurrency and Computation: Practice and Experience*, vol. 23, no. 4, pp. 372-389, 2011.
6. A. Baumgarten, M. Steffen, M. Clausman, and **J. Zambreno**. “A Case Study in Hardware Trojan Design and Implementation”, *International Journal of Information Security (IJIS)*, vol. 10, no. 1, pp. 1-14, 2011.
7. A. Pande and **J. Zambreno**. “Reconfigurable Hardware Implementation of a Modified Chaotic Filter Bank Scheme”, *International Journal of Embedded Systems (IJES)*, vol. 4, no. 3, pp. 248-258, 2010.
8. A. Pande and **J. Zambreno**. “The Secure Wavelet Transform”, *Springer Journal of Real-Time Image Processing (RTIP)*, 2010.
9. A. Baumgarten, A. Tyagi, and **J. Zambreno**. “Preventing Integrated Circuit Piracy using Reconfigurable Logic Barriers”, *IEEE Design and Test of Computers*, vol. 27, no. 1, pp. 66-75, January 2010.
10. G. Bloom, B. Narahari, R. Simha, and **J. Zambreno**. “Protecting Secure Execution Environments with a Last Line of Defense Against Trojan Circuit Attacks”, *Computers and Security*, vol. 28, no. 7, pp. 660-669, October 2009.
11. S. Sun, Z. Yan, and **J. Zambreno**. “Demonstrable Differential Power Analysis Attacks on Real-World FPGA-Based Embedded Systems”, *Integrated Computer-Aided Engineering*, vol. 16, no. 2, pp. 119-130, April 2009.
12. J. Sathre and **J. Zambreno**. “Automated Software Attack Recovery using Rollback and Huddle”, *Springer Journal of Design Automation for Embedded Systems (DAES)*, vol. 12, no. 3, pp. 243-260, September 2008.
13. D. Nguyen, A. Das, **J. Zambreno**, G. Memik, and A. Choudhary. “An FPGA-Based Network Intrusion Detection Architecture”, *IEEE Transactions on Information Forensics and Security (TIFS)*, vol. 3, no. 1, pp. 118-132, March 2008.
14. A. Das, S. Ozdemir, G. Memik, **J. Zambreno**, and A. Choudhary. “Microarchitectures for Managing Chip Revenues under Process Variations”, *IEEE Computer Architecture Letters*, vol. 6, no. 2, pp. 29–32, July 2007.
15. **J. Zambreno**, D. Honbo, A. Choudhary, R. Simha, and B. Narahari. “High-Performance Software Protection using Reconfigurable Architectures”, *Proceedings of the IEEE*, vol. 94, no. 2, pp. 1–13, February 2006.
16. **J. Zambreno**, A. Choudhary, R. Simha, B. Narahari, and N. Memon. “SAFE-OPS: An Approach to Embedded Software Security”, *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 4, no. 1, pp. 189–210, February 2005.

Conference and Workshop Papers

17. A. Pande, P. Mohapatra, and **J. Zambreno**. “Using Chaotic Maps for Encrypting Image and Video Content”, *Proceedings of the International Symposium on Multimedia (ISM)*, December 2011.
18. J. Rilling, D. Graziano, J. Hitchcock, T. Meyer, X. Wang, P. Jones, and **J. Zambreno**. “Circumventing a Ring Oscillator Approach to FPGA-Based Hardware Trojan Detection”, *Proceedings of the International Conference on Computer Design (ICCD)*, October 2011.
19. A. Pande, **J. Zambreno**, and P. Mohapatra. “Hardware Architecture for Simultaneous Arithmetic Coding and Encryption”, *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, July 2011.
20. A. Pande, **J. Zambreno**, and P. Mohapatra. “Architectures for Simultaneous Coding and Encryption using Chaotic Maps”, *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2011. (poster paper)
21. M. Steffen, P. Jones, and **J. Zambreno**. “Teaching Graphics Processing and Architecture using a Hardware Prototyping Approach”, *Proceedings of the International Conference on Microelectronic Systems Education (MSE)*, June 2011.
22. M. Steffen and **J. Zambreno**. “Improving SIMT Efficiency of Global Rendering Algorithms with Architectural Support for Dynamic Micro-Kernels”, *Proceedings of the International Symposium on Microarchitecture (MICRO)*, pp. 237-248, December 2010.
23. A. Pande, **J. Zambreno**, and P. Mohapatra. “Joint Video Compression and Encryption using Arithmetic Coding and Chaos”, *Proceedings of the IEEE International Conference on Internet Multimedia Systems Architecture and Applications (IMSAA)*, December 2010.
24. A. Pande and **J. Zambreno**. “Design and Hardware Implementation of a Chaotic Encryption Scheme for Real-Time Embedded Systems”, *Proceedings of the IEEE Signal Processing and Communications Conference (SPCOM)*, July 2010.
25. M. Steffen and **J. Zambreno**. “A Hardware Pipeline for Accelerating Ray Traversal Algorithms on Streaming Processors”, *Proceedings of the IEEE Symposium on Application Specific Processors (SASP)*, June 2010.
26. M. Karkee, M. Monga, B. Steward, **J. Zambreno**, and A. Kelkar. “Real-Time Simulation and Visualization Architecture with Field Programmable Gate Array (FPGA) Simulator”, *Proceedings of the ASME World Conference on Innovative Virtual Reality (WINVR)*, May 2010.
27. A. Das, G. Memik, **J. Zambreno**, and A. Choudhary. “Detecting/Preventing Information Leakage on the Memory Bus due to Malicious Hardware”, *Proceedings of Design, Automation, and Test in Europe (DATE)*, March 2010.
28. H. Chen, S. Sun, D. Aliprantis, and **J. Zambreno**. “Dynamic Simulation of DFIG Wind Turbines on FPGA Boards”, *Proceedings of the Power and Energy Conference at Illinois (PECI)*, pp. 39-44, February 2010.

29. A. Pande and **J. Zambreno**. “A Reconfigurable Architecture for Secure Multimedia Delivery”, *Proceedings of the International Conference on VLSI Design (VLSID)*, pp. 258-263, January 2010.
30. S. Sun and **J. Zambreno**. “A Floating-point Accumulator for FPGA-based High Performance Computing Applications”, *Proceedings of the International Conference on Field-Programmable Technology (FPT)*, December 2009.
31. E. Leontie, G. Bloom, B. Narahari, R. Simha, and **J. Zambreno**. “Hardware-enforced Fine-grained Isolation of Untrusted Code”, *Proceedings of the Workshop on Secure Execution of Untrusted Code (SecuCode)*, November 2009.
32. J. Sathre, A. Baumgarten, and **J. Zambreno**. “Architectural Support for Automated Software Attack Detection, Recovery, and Prevention”, *Proceedings of the International Conference on Embedded and Ubiquitous Computing (EUC)*, August 2009.
33. A. Pande and **J. Zambreno**. “Efficient Translation of Algorithmic Kernels on Large-Scale Multi-Cores”, *Proceedings of the International Workshop on Reconfigurable and Multicore Embedded Systems (WoRMES)*, August 2009.
34. E. Leontie, G. Bloom, B. Narahari, R. Simha, and **J. Zambreno**. “Hardware Containers for Software Components: A Trusted Platform for COTS-Based Systems”, *Proceedings of the International Symposium on Trusted Computing and Communications (TrustCom)*, August 2009.
35. M. Steffen and **J. Zambreno**. “Design and Evaluation of a Hardware Accelerated Ray Tracing Data Structure”, *Proceedings of Theory and Practice of Computer Graphics (TPCG)*, June 2009.
36. A. Pande and **J. Zambreno**. “An Efficient Hardware Architecture for Multimedia Encryption and Authentication using the Discrete Wavelet Transform”, *Proceedings of the IEEE International Symposium on VLSI (ISVLSI)*, pp. 85-90, May 2009.
37. H. Chen, S. Sun, D. Aliprantis, and **J. Zambreno**. “Dynamic Simulation of Electric Machines on FPGA Boards”, *Proceedings of the IEEE International Electric Machines and Drives Conference (IEMDC)*, May 2009.
38. S. Sun, M. Steffen, and **J. Zambreno**. “A Reconfigurable Platform for Frequent Pattern Mining”, *Proceedings of the International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, December 2008.
39. A. Das, B. Ozisikyilmaz, S. Ozdemir, G. Memik, **J. Zambreno**, and A. Choudhary. “Evaluating the Effects of Cache Redundancy on Profit”, *Proceedings of the International Symposium on Microarchitecture (MICRO)*, November 2008.
40. S. Sun and **J. Zambreno**. “Mining Association Rules with Systolic Trees”, *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, September 2008.

41. A. Pande and **J. Zambreno**. “Polymorphic Wavelet Architectures using Reconfigurable Hardware”, *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, September 2008. (poster paper)
42. A. Pande and **J. Zambreno**. “Design and Analysis of Efficient Reconfigurable Wavelet Filters”, *Proceedings of the IEEE International Conference on Electro/Information Technology (EIT)*, May 2008.
43. S. Sun, J. Yan, and **J. Zambreno**. “Experiments in Attacking FPGA-Based Embedded Systems using Differential Power Analysis”, *Proceedings of the IEEE International Conference on Electro/Information Technology (EIT)*, May 2008.
44. A. Das, S. Misra, **J. Zambreno**, G. Memik, and A. Choudhary. “An Efficient FPGA Implementation of Principle Component Analysis-based Network Intrusion Detection System”, *Proceedings of Design, Automation, and Test in Europe (DATE)*, March 2008.
45. S. Pati, R. Narayanan, G. Memik, A. Choudhary, and **J. Zambreno**. “Design and Implementation of an FPGA Architecture for High-Speed Network Feature Extraction”, *Proceedings of the International Conference on Field-Programmable Technology (ICFPT)*, pp. 49–56, December 2007.
46. J. Sathre and **J. Zambreno**. “Rollback and Huddle: Architectural Support for Trustworthy Application Replay”, *Proceedings of the Workshop on Embedded Software Security (WESS)*, October 2007.
47. A. Das, S. Ozdemir, G. Memik, **J. Zambreno**, and A. Choudhary. “Mitigating the Effects of Process Variation: Architectural Approaches for Improving Batch Performance”, *Proceedings of the Workshop on Architectural Support for Gigascale Integration (ASGI)*, June 2007.
48. R. Narayanan, B. Ozisikyilmaz, G. Memik, A. Choudhary, and **J. Zambreno**. “Quantization Error and Accuracy-Performance Tradeoffs for Embedded Data Mining Workloads”, *Proceedings of the International Workshop on High Performance Data Mining (HPDM)*, pp. 734–741, May 2007.
49. R. Narayanan, D. Honbo, G. Memik, A. Choudhary, and **J. Zambreno**. “An FPGA Implementation of Decision Tree Classification”, *Proceedings of Design, Automation, and Test in Europe (DATE)*, pp. 189–194, April 2007.
50. A. Choudhary, R. Narayanan, B. Ozisikyilmaz, G. Memik, **J. Zambreno**, and J. Pisharath. “Optimizing Data Mining Workloads using Hardware Accelerators”, *Proceedings of the Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW)*, February 2007.
51. B. Ozisikyilmaz, R. Narayanan, **J. Zambreno**, G. Memik, and A. Choudhary. “An Architectural Characterization Study of Data Mining and Bioinformatics Workloads”, *Proceedings of the IEEE International Symposium on Workload Characterization (IISWC)*, pp. 61–70, October 2006.

52. R. Narayanan, B. Ozisikyilmaz, **J. Zambreno**, G. Memik, and A. Choudhary. "MineBench: A Benchmark Suite for Data Mining Workloads", *Proceedings of the IEEE International Symposium on Workload Characterization (IISWC)*, pp. 182–188, October 2006.
53. R. Simha, B. Narahari, **J. Zambreno**, and A. Choudhary. "Secure Execution with Components from Untrusted Foundries", *Proceedings of the Advanced Networking and Communications Hardware Workshop (ANCHOR)*, June 2006.
54. J. Pisharath, **J. Zambreno**, B. Ozisikyilmaz, and A. Choudhary. "Accelerating Data Mining Workloads: Current Approaches and Future Challenges in System Architecture Design", *Proceedings of the International Workshop on High Performance Data Mining (HPDM)*, April 2006.
55. **J. Zambreno**, B. Ozisikyilmaz, J. Pisharath, G. Memik, and A. Choudhary. "Performance Characterization of Data Mining Applications using MineBench", *Proceedings of the Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW)*, February 2006.
56. **J. Zambreno**, T. Anish, and A. Choudhary. "A Run-Time Reconfigurable Architecture for Embedded Program Flow Verification", *Proceedings of the NATO Advanced Research Workshop (ARW) on Security and Embedded Systems*, August 2005.
57. O. Gelbart, P. Ott, B. Narahari, R. Simha, A. Choudhary, and **J. Zambreno**. "CODESSEAL: A Compiler/FPGA Approach to Secure Applications", *Proceedings of the IEEE International Conference on Intelligence and Security Informatics (ISI)*, pp. 530–535, May 2005.
58. K. Mohan, B. Narahari, R. Simha, P. Ott, A. Choudhary, and **J. Zambreno**. "Performance Study of a Compiler/Hardware Approach to Embedded Systems Security", *Proceedings of the IEEE International Conference on Intelligence and Security Informatics (ISI)*, pp. 543–548, May 2005.
59. **J. Zambreno**, D. Honbo, and A. Choudhary. "Exploiting Multi-Grained Parallelism in Reconfigurable SBC Architectures", *Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 333–334, April 2005. (poster paper)
60. R. Simha, A. Choudhary, B. Narahari, and **J. Zambreno**. "An Overview of Security-Driven Compilation", *Proceedings of the Workshop on New Horizons in Compiler Analysis and Optimizations*, December 2004.
61. D. Nguyen, **J. Zambreno**, and G. Memik. "Flow Monitoring in High-Speed Networks with 2D Hash Tables", *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, pp. 1093–1097, August 2004. (poster paper)
62. **J. Zambreno**, D. Nguyen and A. Choudhary, "Exploring Area/Delay Tradeoffs in an AES FPGA Implementation". *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, pp. 575–585, August 2004.

63. **J. Zambreno**. “Design and Evaluation of an FPGA Architecture for Software Protection”, *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, p. 1180, August 2004. (poster paper)
64. **J. Zambreno**, R. Simha, and A. Choudhary. “Addressing Application Integrity Attacks using a Reconfigurable Architecture”, *Proceedings of the ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 2004. (poster paper)
65. **J. Zambreno**, A. Choudhary, R. Simha, and B. Narahari. “Flexible Software Protection using Hardware/Software Codesign Techniques”, *Proceedings of Design, Automation, and Test in Europe (DATE)*, pp. 636–641, February 2004.
66. M. Kandemir, I. Kadayif, A. Choudhary, and **J. Zambreno**. “Optimizing Inter-processor Data Locality”, *Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 127–135, October 2002.
67. **J. Zambreno**, M. Kandemir, and A. Choudhary. “Enhancing Compiler Techniques for Memory Energy Optimizations”, *Proceedings of the International Conference on Embedded Software (EMSOFT)*, pp. 364–381, October 2002.

Other Papers

66. **J. Zambreno**. *Compiler and Architectural Approaches to Software Protection and Security*. Ph.D. Thesis, Northwestern University, June 2006.
67. **J. Zambreno**. *Enhancing Compiler Techniques for Memory Energy Optimizations*. M.S. Thesis, Northwestern University, June 2001.

INVITED TALKS

- **J. Zambreno**. “Architectural Approaches to Embedded Program Flow Protection”, Motorola Workshop on Security (held at Northwestern University), October 2006.
- **J. Zambreno**. “Protecting Critical Computing Systems: A Hardware/Software Codesign Approach”, ECE Department, University of Pittsburgh, April 2006.
- **J. Zambreno**. “Protecting Critical Computing Systems: A Hardware/Software Codesign Approach”, ECE Department, Texas A&M University, March 2006.
- **J. Zambreno**. “Protecting Critical Computing Systems: A Hardware/Software Codesign Approach”, ECE Department, Virginia Tech University, March 2006.
- **J. Zambreno** and B. Narahari. “Protecting Critical Computing Systems: A Hardware/Software Codesign Approach”, Institute for Defense Analyses, March 2006.
- **J. Zambreno**. “Protecting Critical Computing Systems: A Hardware/Software Codesign Approach”, CS Department, Colorado State University, February 2006.
- **J. Zambreno**. “Protecting Critical Computing Systems: A Hardware/Software Codesign Approach”, ECE Department, Clemson University, February 2006.
- **J. Zambreno**. “Protecting Critical Computing Systems: A Hardware/Software Codesign Approach”, ECpE Department, Iowa State University, February 2006.

- **J. Zambreno** and A. Choudhary. “Hardware/Software Co-Design for System Security”, Institute for Defense Analyses (DARPA Workshop on Research Opportunities for Trusted ICs), August 2005.

SPONSORED RESEARCH FUNDING

External Funding

- “CSR:Small:Hardware Architectures for Data Mining at the Exascale” (PI). *National Science Foundation (NSF), Computer Systems Research Program*. Total funding - \$449,998, 2011–2014.
- “An Adaptive Property-Aware HW/SW Framework for DDDAS” (Co-PI with P. Jones, N. Elia, R. Cytron, and C. Gill). *Air Force Office of Scientific Research (AFOSR), Dynamic Data Driven Application Systems Program*. Total funding - \$299,987 (ISU share, \$168,656), 2011–2013.
- “EAGER:Collaborative Research:Seamless Integration of Conjoined Cyber-Physical System Properties” (Co-PI with P. Jones, R. Cytron, and C. Gill). *National Science Foundation (NSF), Cyber-Physical Systems Program*. Total funding - \$299,917 (ISU share, \$149,928), 2010–2012.
- “CT-M: Hardware Containers for Software Components - Detection and Recovery at the Hardware/Software Interface” (Co-PI with R. Simha, B. Narahari, and A. Choudhary). *National Science Foundation (NSF), CyberTrust Program*. Total funding - \$980,000 (ISU share - \$200,000 + \$16,000 REU supplement), 2009–2012.
- “Architectural Support for Detection and Recovery using Hardware Wrappers” (Co-PI with B. Narahari and R. Simha). *Air Force Office of Scientific Research (AFOSR)*. Total funding - \$479,390 (ISU share - \$172,083), 2009–2012.

Equipment and Software

- Donation of 14 DIGILAB-XUP-V5 boards. *Xilinx University Program*. Total commercial value - \$27,986, 2010.
- Donation of 15 Virtex 5 FPGAs for use in high performance reconfigurable computing platform. *Xilinx University Program*. Total commercial value - \$57,268, 2010.
- Donation of 2 XUPV5-LX110T boards. *Xilinx University Program*. Total commercial value - \$3,998, 2009.
- “A Strategic Vision for Autonomous Vehicle Research at Iowa State University” (PI with A. Stoytchev and A. Tyagi). *ECpE Strategic Planning and Execution Committee, Iowa State University*. Total funding - \$25,000, 2008.
- “Comparative Studies on Using Multi-Core Processors in High-Performance Computing and Emerging Applications” (Co-PI with M. Chang, M. Sosonkina, and Z. Zhang). *ECpE Strategic Planning and Execution Committee, Iowa State University*. Total funding - \$30,500, 2008.
- Donation of 16 Virtex 4 FPGAs for use in logic emulation platform. *Xilinx University Program*. Total commercial value - \$75,000, 2007.
- “Laboratory for Trusted Embedded Systems” (Co-PI with T. Daniels, A. Tyagi, and Z. Zhang). *ECpE Strategic Planning Committee, Iowa State University*. Total funding - \$50,000, 2007.

Internal Funding

- “Enabling Real-time Vehicle Simulation with VR Interface using HW/SW Accelerators” (PI with B. Steward and A. Kelkar). *Information Infrastructure Institute (ICube)*, Iowa State University. Total funding - \$5,000, 2010.
- “Real-Time Management of Integrated Information, Physical, and Human Networks” (Co-PI with P. Jones). *Information Infrastructure Institute (ICube)*, Iowa State University. Total funding - \$5,000, 2009.
- “Enhancing Realism and Flexibility of VR-Based Real-Time Dynamic Simulation Framework with Operator and Hardware-in-the-loop Interface” (Collaborator with A. Kelkar and B. Steward). *Virtual Reality Applications Center (VRAC)*, Iowa State University. Personal share of funding - \$50,000, 2008–2010.
- “Acceleration and Efficiency Exploration of Cryptographic Kernels on Multi-Core Processing Platforms” (PI). *Center for Information Protection (CIP)*, Iowa State University. Total funding - \$25,000, 2007–2008.
- “CODELESS: COnfigurable DEvices for Large-scale Energy System Simulation” (Co-PI with D. Aliprantis). *Information Infrastructure Institute (ICube)* and *Electric Power Research Center (EPRC)*, Iowa State University. Total funding - \$29,000, 2008–2009.
- “Architectural Approaches to Embedded Program Flow Protection” (PI). *Center for Information Protection (CIP)*, Iowa State University. Total funding - \$25,000, 2006–2007.

STUDENT SUPERVISION

Current Students

- Michael Steffen, Ph.D. student
- Ravi Yasa, Ph.D. student
- Xinying Wang, Ph.D. student
- Lakshmi Tondehal, M.S. student
- Michael Patterson, M.S. student
- Aaron Mills, M.S. student
- Jacob Bower, M.S. student

Previous Students

- Song Sun, Ph.D. 2011, *Analysis and Acceleration of Data Mining Algorithms on High Performance Reconfigurable Computing Platforms*
- Amit Pande, Ph.D. 2010, *Algorithms and Architectures for Secure Embedded Multimedia Systems*
- Justin Rilling, M.S. 2011, *Persistent Monitoring of Digital ICs to Verify Hardware Trust*
- Madhu Monga, M.S. 2010, *Real-Time Simulation of Dynamic Vehicle Models using High Performance Reconfigurable Computing Platforms*
- Joel Millage, M.S. 2010, *GPU Integration into a Software Defined Radio Framework*
- Dustin Counsell, M.S. 2010, *Evaluation of High-Level Hardware/Software Embedded System Design Flows*
- Jacob Braegelmann, M.S. 2009, *An Independent Analysis of High-Level System Modeling and Design Languages*

- Alex Baumgarten, M.S. 2009, *Preventing Integrated Circuit Piracy using Reconfigurable Logic Barriers*
- Jesse Sathre, M.S. 2008, *Architectural Support for Secure and Survivable Software*

Graduate Student Committees

- Ph.D. committees: Ramon Mercado (advisor - D. Rover), Pubali Banerjee (advisor - D. Jacobson), Zhongbo Cao (advisor - D. Rover), Viswanathan Subramanian (advisor - A. Somani), Dan Gieseeman (advisor - T. Daniels), Abhinav Sarje (advisor - S. Aluru), Bashar Gharaibeh (advisor - M. Chang), Michael Frederick (advisor - A. Somani), Prem Ramesh (advisor - A. Somani), Zijun Yan (advisor - C. Chu), Benjamin Jackson (advisor - S. Aluru), Sharhabeel Al Nabelsi (advisor - A. Kamal), Abhishek Das (Northwestern University, advisor - A. Choudhary), Hao Chen (advisor - D. Aliprantis), Pavan Kumar (advisor - A. Somani), Tyler Sondag (advisor - H. Rajan), Yanan Cao (advisor - Z. Zhang), Zhiming Zhang (advisor - M. Chang)
- M.S. committees: Andrew Riha (advisor - D. Rover), Kenneth McVicker (advisor - D. Jacobson), Jeffrey Schmidt (advisor - Z. Zhang), Bharath Karthik (advisor - R. Geiger), Preethika Kalyanasundaram (advisor - G. Manimaran), Adwait Gupte (advisor - P. Jones), Yang Yang (advisor - T. Daniels), Pooja Mhapsekar (advisor - P. Jones), Wade Paustian (advisor - T. Daniels), Moin Sayed (advisor - P. Jones), T. Meyer (advisor - Y. Guan), D. Graziano (advisor - T. Daniels)

Undergraduate Student Supervision

- Christopher Sabotta, 2011
- Kyle Peterson, 2011
- Max Mayfield, 2011 (REU)
- Kevin Pope, 2011 (REU)
- Taehyun Park, 2010
- Jamin Hitchcock, 2010
- Mikhail Drob, 2010 (REU)
- Michael Patterson, 2010 (REU)
- Stephen LeBlanc, 2010 (Freshman Honors program)
- Abhishek Vemuri, 2010 (Freshman Honors program)
- Michael Carter, 2010 (Freshman Honors program)
- Bailey Steinfadt, 2010
- Greg Hogan, 2010
- Christopher Morgan, 2009 (Freshman Honors program)
- Gregory Gholson, 2009 (Freshman Honors program)
- Michael Svendsen, 2008 (Freshman Honors program)
- Dave Peters, 2008 (Freshman Honors program)
- Tim Meyer, 2007–2008 (Freshman Honors program)
- Cole Anagnost, 2007 (Freshman Honors program)

Senior Design Supervision

- Kevin Pope, Steven Bruening, MatthewDavid Grove, Max Mayfield, Michael Yeager, “Virtual Pinball Experience”, 2011–2012
- Brandon Otto, Jonathan Henze, Kevin Moore, Marvin Toeung, Richard Rojas, “Multi-Arcade Emulation System”, 2011–2012
- David Gartner, John Alexander, Danny Funk, Tony Milosch, Cory Mohling. “FPGA-based Arcade Emulation System”, 2010–2011
- Ashley Good, David Graziano, Tim Meyer, Matt Saladin. “FPGA-based Emulation of the Nintendo Entertainment System”, 2009–2010
- Adam Ahrens, Amelia Gee, Joshua Mensah, Jonathan Salvador, Bailey Steinfadt. “College of Engineering iPhone Application”, 2009–2010
- Derek Baldus, Greg Hogan, David Kaiser, Scott Penick. “Web-based Thermostat Control System”, 2008–2009
- Alex Burds, Jin-Ning Tioh, Tony Ross, Dave Zajicek. “Logic Design Training Tool”, 2007–2008
- Brendan Campbell, Sean Godinez, Daniel Risse, Aaron Westphal. “CyRay: An Interactive Ray Tracer for the PlayStation 3”, 2007–2008

Supervised Student Awards

- Michael Patterson, Christopher Sabotta, Sudhanshu Vyas, and Aaron Mills, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 2nd place entry, 2011
- Amit Pande, *Zaffarano Prize for Graduate Research Research* (honorable mention), 2011
- Amit Pande, *Iowa State University Research Excellence Award (REA)*, 2010
- Amit Pande, *CRA/CCC Computing Innovation Fellow* (post-doctoral fellowship sponsored by NSF), 2010
- Michael Steffen and Veerendra Allada, *ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) Design Contest*, 5th place entry, 2010
- David Graziano, Tim Meyer, Jamin Hitchcock, Xinying Wang, and Justin Rilling, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 2nd place entry, 2010
- Michael Steffen and Justin Rilling, *ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) Design Contest*, 2nd place entry (performance category), 2009
- Amit Pande, *International Conference on VLSI Design (VLSID) Design Contest*, 3rd place entry, 2009
- Alex Baumgarten and Michael Steffen, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 1st place entry, 2008
- Michael Steffen, *National Science Foundation (NSF) Graduate Research Fellowship*, 2008–2011
- Michael Steffen, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 3rd place entry, 2007
- Jesse Sathre, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 2nd place entry, 2007
- Tim Meyer, *University Honors Summer Research Grant*, 2007

UNIVERSITY SERVICE

- 2011–2012 Member, ECpE Curriculum Committee
- 2011–2012 Member, ECpE Student Professional Development Committee
- 2010–2011 Member, ECpE Promotion and Tenure Committee
- 2009–2010 Member, ECpE Senior Design Committee
- 2009–2011 Member, ECpE Graduate Committee
- 2009–2011 Chair, ECpE Computing and Networking Systems Group
- 2009–2011 Volunteer, IT Olympics Competition
- 2009–2011 Mentor, Engineering Leadership Program
- 2008–2010 Member, ECpE Chair Search Committee
- 2008–2010 Member, ECpE Elections and Oversight Committee
- 2008–2009 Member, ECpE Undergraduate Recruiting Committee
- 2007–2009 Member, ECpE Strategic Planning and Execution Committee
- 2007–2009 Member, ECpE Curriculum Committee
- 2006–2008 Member, ECpE Graduate Admissions Committee
- Spring 2007 Judge, ECpE EAB poster competition
- Spring 2008 Judge, Iowa State Science and Technology Fair
- Spring 2007 Judge, Iowa State Science and Technology Fair
- 2006–2010 Participant, Meet-A-Professor-At-Lunch (MAPAL) program