$g_m/I_D$ based Two-Stage Amplifier Design

Chongli Cai

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Motivation

- $I_d/(W/L)$ VS $V_G$ is sensitive to $V_{bs}$
Motivation

- $gm/Id$ vs $VG$ is also sensitive to $Vbs$
Motivation

- But $gm/ID$ vs $ID/(W/L)$ has fixed shape

Let's look at the $gm/Id$ curve of the model we are using in the lab

- With a certain current density, the $gm/id$ value is fixed regardless of $Vbs$
Design Tradeoff: $g_m/I_D$ and $f_T$

- Weak inversion: Large $g_m/I_D (>20 \text{S/A})$, but small $f_T$
- Strong inversion: Small $g_m/I_D (<5 \text{S/A})$, but large $f_T$
The product of $\frac{g_m}{I_D}$ and $f_T$ peaks in moderate inversion. Operating the transistor in moderate inversion is optimal when we value speed and power efficiency equally. But not always the case!
Why $g_m/I_D$ is important?

- $g_m/|D$ curve is generated from SPICE simulation, which is linked to the actual measurement data
  - Better match to the fabricated one

- $g_m/|d$ value does not rely on any model equation
  - Avoid the design uncertainties

- $g_m/|d$ Value has fixed shape regardless of transistor length

- $g_m/|d$ curve is valid all over the transistor operating range

- $g_m/|d$ method can reduce the design and optimization effort a lot
  - Once selecting one point from $g_m/|d$ curve, with another design parameter the third parameter can be easily determined
  - Example:

\[
\begin{align*}
\frac{g_m}{I_D} & \Rightarrow g_m \\
\frac{I_d}{I_{du}} & \Rightarrow \frac{W}{L} \\
\frac{W}{L} & \Rightarrow I_d
\end{align*}
\]
How $g_m/I_D$ related to Design Specification?

- **Design Specification**
  - GBW, SR, phase margin, power and area etc.
  - \[
  GBW = \frac{1}{2} \left( \frac{g_{m1}}{I_{D1}} \right) = \frac{1}{2} \left( \frac{g_{m1}}{I_{D1}} \right) \cdot SR \\
  \]
  - \[
  SR_i = \frac{2I_{D1}}{C_c} \\
  SR_{II} = \frac{1}{2} \frac{I_{D6}}{C_L + C_c} \\
  \]

- \[
  C_L \]
  - \[
  PM = 90^\circ - \tan^{-1} \left( \frac{2g_{m1}}{g_{m6}/I_{D6}} \right) \cdot \left[ \frac{C_L C_{o1} + C_L C_c + C_c C_{o1}}{C_c^2} \right] - \tan^{-1} \left( \frac{g_{m1}/I_{D1}}{g_{m6}/I_{D6}} \right) \cdot \left( \frac{C_L}{C_c} \right) \\
  \]

- You will not gain more benefits on making M6 much larger
- It is better to select the $g_m/i_d$ value of M6 to make it operating in the moderate inversion.
- So it is valid to assume $C_{o1}$ is smaller than $C_L$ in the design.

The PM can be simplified as

\[
PM = 90^\circ - \tan^{-1} \left( \frac{g_{m1}/I_{D1}}{g_{m6}/I_{D6}} \cdot C_L \right) - \tan^{-1} \left( \frac{g_{m1}/I_{D1}}{g_{m6}/I_{D6}} \cdot \frac{C_L}{C_c} \right) \\
\]

**Note:** $k = \frac{g_{m1}/I_{D1}}{g_{m6}/I_{D6}}$

\[
PM = 90^\circ - \tan^{-1} \left( k \cdot \frac{I_{D1}}{I_{D6}} \cdot C_L \right) - \tan^{-1} \left( k \cdot \frac{I_{D1}}{I_{D6}} \cdot \frac{C_L}{C_c} \right) \\
\]
**How $g_{m}/I_D$ related to Design Specification?**

- Phase Margin = 60°

\[
PM = 90^\circ - \tan^{-1}(k \cdot \frac{I_{D1}}{I_{D6}} + \frac{C_L}{C_c}) - \tan^{-1}(k \cdot \frac{I_{D1}}{I_{D6}})
\]

\[
k \left(1 + \frac{C_L}{C_c} \right) \left( \frac{I_{D1}}{I_{D6}} \right) \left(1 - k^2 \left( \frac{C_L}{C_c} \right)^2 \left( \frac{I_{D1}}{I_{D6}} \right)^2 \right)
\]

with the condition of

\[
SR_I \leq SR_{II} \Rightarrow \frac{I_{D1}}{I_{D6}} \leq \frac{C_c}{2(C_L + C_c)} \quad (1)
\]

\[
\sqrt{3}k \left(1 + \frac{C_L}{C_c} \right) \left( \frac{I_{D1}}{I_{D6}} \right) = 1 - k^2 \left( \frac{C_L}{C_c} \right)^2 \left( \frac{I_{D1}}{I_{D6}} \right)^2 \quad (2)
\]

- $k$ is determined by the $g_{m}/I_D$ value of M1 and M6 you choose
- $I_{D1}/I_{D6}$ can be determined in terms of total power consumption
- Once $k$ and current ratio are chosen, then $C_c$ is determined
- You need to use (1) to check the validity of the calculated $C_c$ from (2)
- You need to keep observing the parasitic cap at gate of M6 to make sure it is small

**Equations**

- \[
g_{m1} = \frac{2GBW}{SR}
\]
- \[
SR_I = \frac{2I_{D1}}{C_c}
\]
- \[
SR_{II} \geq \frac{I_{D6}}{C_L + C_c}
\]
- \[
k = \frac{g_{m1}/I_{D1}}{g_{m6}/I_{D6}}
\]
## Design Guideline

### Amplifier Design Procedure

<table>
<thead>
<tr>
<th>Step</th>
<th>Equation/Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( g_{m1}/I_{D1} )</td>
</tr>
<tr>
<td>2</td>
<td>( g_{m6}/I_{D6} )</td>
</tr>
<tr>
<td>3</td>
<td>( I_{D1}/I_{D6} \leq \frac{C_c}{2(C_L + C_c)} )</td>
</tr>
<tr>
<td>4</td>
<td>Calculate ( C_c )</td>
</tr>
<tr>
<td>5</td>
<td>Check the validity of ( C_c )</td>
</tr>
<tr>
<td>6</td>
<td>Size M1 &amp; M6</td>
</tr>
<tr>
<td>7</td>
<td>Size M3 &amp; M4</td>
</tr>
<tr>
<td>8</td>
<td>Size M5 &amp; M7</td>
</tr>
</tbody>
</table>

- \( g_{m1} \): Transconductance of the first stage
- \( I_{D1} \): Drain current of the first stage
- \( I_{D6} \): Drain current of the sixth stage
- \( C_c \): Capacitance
- \( C_L \): Load capacitance
- \( C_c \): Coupling capacitance
- \( I_{bias} \): Bias current
- \( V_{DD} \): Power supply
- \( V_{ss} \): Ground
- \( V_{in} \): Input voltage
- \( V_{out} \): Output voltage
- \( W/L \): Width/Length ratio
- \( k \): Constants

![Amplifier Circuit Diagram]
# Design Example – Specification

<table>
<thead>
<tr>
<th>Specs</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>+/- 2.5V</td>
</tr>
<tr>
<td>Load Capacitor</td>
<td>2pF</td>
</tr>
<tr>
<td>Total Current</td>
<td>&lt;=100uA</td>
</tr>
<tr>
<td>DC Gain</td>
<td>75dB</td>
</tr>
<tr>
<td>Gain-bandwidth-product</td>
<td>25MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>60°</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>25MV/s</td>
</tr>
</tbody>
</table>
Target: GBW=25MHz; SR=25V/us

Pick-up point in moderate inversion region

Final Value will be slightly larger due to parasitic caps

Valid

1) In this case, GBW and SR are choose to be barely on the design target

$$\text{GBW} = \frac{1}{2} \left( \frac{g_{m1}}{I_{D1}} \right) * \text{SR}$$

- You can choose the gm1/id1 to make GBW and SR barely satisfy the target
- For SR is barely at target value, choosing a large gm1/id1 can result in GBW over-designed
- For GBW is barely at target value, choosing small gm1/id1 can result in SR over-designed

2) Choosing $k = 1$, then $\frac{g_{m1}}{I_{D1}} = 12.56$

3) Choosing $\frac{I_{D1}}{I_{D6}} = 0.1$

4) Calculate $C_c = 443 \text{fF}$

5) Checking $\left( \frac{I_{D1}}{I_{D6}} = 0.1 \right) \leq \left( \frac{C_c}{2(C_L + C_c)} \approx 0.1 \right)$
Design Step 6

**NMOS**

\[
\begin{align*}
I_6 &= 75 \mu A \\
I_{du6} &= 1.97 \mu A^{-1} \Rightarrow \left(\frac{W}{L}\right)_6 = 38
\end{align*}
\]

**PMOS**

\[
\begin{align*}
I_1 &= 7.5 \mu A \\
I_{du1} &= 0.471 \mu A^{-1} \Rightarrow \left(\frac{W}{L}\right)_1 = 16
\end{align*}
\]
Design Step 7 & 8

- M3 and M4 need to have over-drive voltage in the range of 200mV to 300mV
- For the Top three transistors M5-M7, the over-drive voltage is set to be 300mV~400mV for the purpose of reducing current mismatch, and the Vds need to be large (usually Vds>=1.5*Vod)
### Simulated Result

The design is essentially “right on” the target without any tweaking.

<table>
<thead>
<tr>
<th>Specs</th>
<th>Specification</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>+/- 2.5V</td>
<td>+/-2.5V</td>
</tr>
<tr>
<td>Total Current</td>
<td>&lt;=100uA</td>
<td>90uA</td>
</tr>
<tr>
<td>DC Gain</td>
<td>75dB</td>
<td>77dB</td>
</tr>
<tr>
<td>Gain-bandwidth-product</td>
<td>25MHz</td>
<td>25MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>60°</td>
<td>61°</td>
</tr>
<tr>
<td>Slew Rate: SR +/-</td>
<td>25MV/s</td>
<td>22.37/25.9 MV/s</td>
</tr>
</tbody>
</table>
Loop Stability Simulation

- Using stb analysis in close-loop
Slew Rate Simulation

- M4: 1.510097us, 998.6579mV
- M5: 1.58738us, -1.004786V
- M6: 1.58738us, -1.004786V
- dx: 89.66008ns, dy: 2.001017V, s: 22.31781MV/s
- dx: 77.28257ns, dy: 2.003444V, s: 25.92362MV/s
Conclusion

- The key advantage of gm/Id based design is that it allows you to transition from hand analysis to Spice simulation without much of modelling uncertainties
  - Because we are incorporating the relevant simulation data into the design process.
- The simulation result of gm/Id based design can match the fabricated circuit well
  - Because the gm/id directly carries on the device measurement information
Questions?