

# CLOSED FORM SOLUTION TO SIMULTANEOUS BUFFER INSERTION/SIZING AND WIRE SIZING\*

Chris C. N. Chu and D. F. Wong  
*cnchu@cs.utexas.edu and wong@cs.utexas.edu*

Department of Computer Sciences, University of Texas at Austin, Austin, TX 78712.

## ABSTRACT

In this paper, we consider the delay minimization problem of a wire by simultaneously considering buffer insertion, buffer sizing and wire sizing. We consider three versions of the problem, namely using no buffer, using a given number of buffers, and using optimal number of buffers. We provide elegant closed form optimal solutions for all these versions.

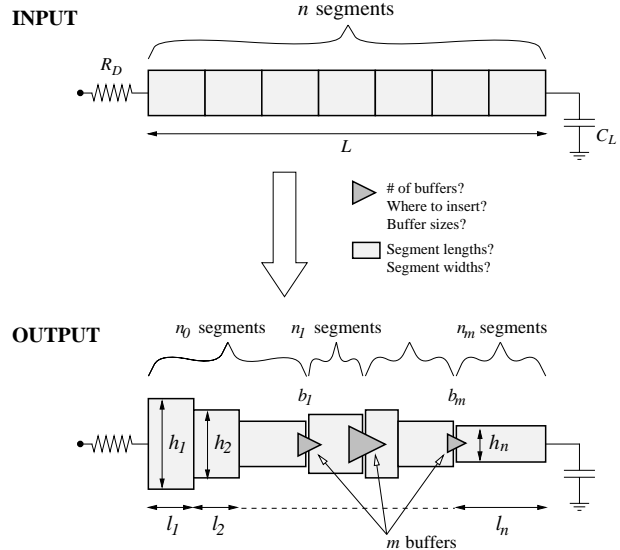
## 1. INTRODUCTION

As VLSI technology continues to scale down, interconnect delay has become the dominant factor in deep submicron design. Recently, many works have been done on buffer insertion, buffer sizing and/or wire sizing in order to reduce the interconnect delay (e.g. [1, 2, 3, 4, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16]). Currently, the best solutions to the buffer insertion, buffer sizing and/or wire sizing problems are either iterative algorithms which locally optimize the size of a wire segment or the size of a buffer at each step, or by dynamic programming. However, both approaches require long running time and large amount of memory in order to have accurate results.

In this paper, we consider the delay minimization problem of a wire by simultaneously considering buffer insertion, buffer sizing and wire sizing. Given the length of the wire, the driver resistance and load capacitance, we are allowed to divide the wire into segments and to optionally insert buffers between any two adjacent segments. The sizes of buffers and the lengths and widths of segments can all be changed in order to minimize the delay from source to sink. Note that wire sizing we are considering here is more general than those in previous works as the lengths of segments can also be varied, as long as the total length is  $L$ . The buffer insertion problem is also different as buffers can be inserted anywhere, rather than having some pre-defined candidate buffer locations.

We solve several variants of this problem. We call the most sophisticated version of it BISWIS (simultaneous Buffer Insertion/Sizing and Wire Sizing problem), which can be defined formally as follows: The input is the length of the wire  $L$ , the driver resistance  $R_D$ , the load capacitance  $C_L$  (together with other electrical parameters) and the total number of segments  $n$  to be used. The output variables are listed

below. Let  $m$  be the number of buffers used. (Therefore the wire is separated by the buffers into  $m + 1$  pieces). For  $0 \leq j \leq m$ , let  $n_j$  be the number of segments between the  $j$ th buffer and the  $(j + 1)$ th buffer (with  $n_0$  being the number of segments between the source and the first buffer and  $n_m$  being the number of segments between the last buffer and the sink). For  $1 \leq j \leq m$ , let  $b_j$  be the size of the  $j$ th buffer. For  $1 \leq i \leq n$ , let  $l_i$  and  $h_i$  be the length and width of the  $i$ th segment respectively. The objective is to minimize the delay  $D$  from source to sink over  $m$ ,  $n_0, \dots, n_m$ ,  $b_1, \dots, b_m$ ,  $l_1, \dots, l_n$  and  $h_1, \dots, h_n$  simultaneously, with constraints  $n_0 + \dots + n_m = n$  and  $l_1 + \dots + l_n = L$ . We give a closed form optimal solution to this problem. See Figure 1 for an illustration of BISWIS.



**Figure 1.** Illustration of the BISWIS problem. The input is  $L, R_D, C_L$  and  $n$ . The output is  $m, n_0, \dots, n_m, b_1, \dots, b_m, l_1, \dots, l_n$  and  $h_1, \dots, h_n$ . We provide a closed form optimal solution of it which minimizes the delay.

Note that  $n$  is a parameter that allows us to determine how good the solution will be. We can get a smaller delay by using a larger value of  $n$ .

In order to solve BISWIS, we first consider two simpler variants of it. The first one is that no buffer is allowed. Therefore, this is the problem of delay minimization by wire sizing alone. We call this version WIS (Wire Sizing problem). The second variant is that the number of buffers  $m$  is given as input. The objective is to minimize  $D$  over  $n_0, \dots, n_m, b_1, \dots, b_m, l_1, \dots, l_n$  and  $h_1, \dots, h_n$  simultaneously, with constraints  $n_0 + \dots + n_m = n$  and  $l_1 + \dots + l_n = L$ . We call this version BISWIS/ $m$  (simultaneous Buffer Insertion/Sizing and Wire Sizing problem with  $m$  buffers).

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These two problems are key intermediate steps to solve BISWIS. They are also very interesting practically by themselves. Because instead of using the optimal number of buffers, we may want to use less or not to use any at all. In these cases, we will need these simpler versions. We provide closed form optimal solutions for both of them.

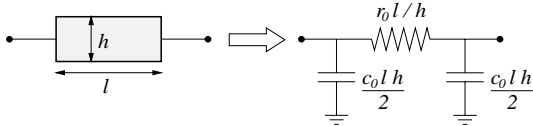
The remainder of this paper is organized as follows: In Section 2, we will consider WIS. The closed form solution is summarized in Theorem 1. In Section 3, we will consider BISWIS/ $m$ . The closed form solution is summarized in Theorem 2. Then in Section 4, by showing how to find the optimal number of buffers, we give a closed form solution for BISWIS. The result is summarized in Theorem 3. In Section 5, we will discuss some interesting observations and implications of our results. We will also discuss how to extend our results to handle nets with tree topology and to handle wire fringing capacitance.

Many proofs in this paper contain a lot of tedious manipulation of complicated mathematical expressions and so only proof outlines are given due to space limitation. Please read [5] for proof details.

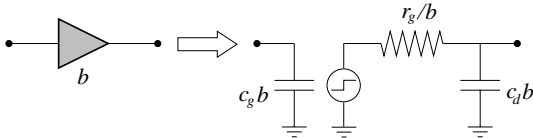
The following are the notations of the electrical parameters used in this paper:

- $R_D$ : Driver resistance.
- $C_L$ : Load capacitance.
- $r_0$ : Unit wire resistance.
- $c_0$ : Unit wire area capacitance.
- $c_g$ : Unit gate capacitance of buffer.
- $r_g$ : Unit gate resistance of buffer.
- $c_d$ : Unit diffusion capacitance of buffer.

Elmore delay model [10] is used here for delay calculation. A wire segment is modeled as a  $\pi$ -type RC circuit as shown in Figure 2. A buffer is modeled as a switch-level RC circuit as shown in Figure 3.



**Figure 2.** The model of a wire segment of length  $l$  and width  $h$  by a  $\pi$ -type RC circuit.



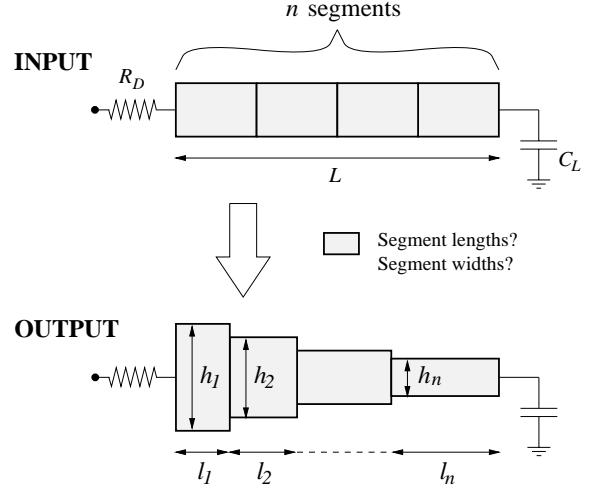
**Figure 3.** The model of a buffer of size  $b$  by a switch-level RC circuit.

## 2. WIRE SIZING

In this section, we consider the case when no buffer is used. Therefore, we consider the delay minimization problem from source to sink by sizing the  $n$  segments of the wire. We call this the WIS problem. See Figure 4 for an illustration.

The delay  $D$  can be written as a function of  $l_i$ 's and  $h_i$ 's:

$$D = R_D(c_0 l_1 h_1 + c_0 l_2 h_2 + \cdots + c_0 l_n h_n + C_L) + \frac{r_0 l_1}{h_1} \left( \frac{c_0 l_1 h_1}{2} + c_0 l_2 h_2 + \cdots + c_0 l_n h_n + C_L \right)$$



**Figure 4.** Illustration of the WIS problem. The input is  $L, R_D, C_L$  and  $n$ . The output is  $l_1, \dots, l_n$  and  $h_1, \dots, h_n$ . We provide a closed form optimal solution of it which minimizes the delay.

$$+ \frac{r_0 l_2}{h_2} \left( \frac{c_0 l_2 h_2}{2} + \cdots + c_0 l_n h_n + C_L \right) + \vdots + \frac{r_0 l_n}{h_n} \left( \frac{c_0 l_n h_n}{2} + C_L \right) \quad (1)$$

We want to minimize  $D$  with respect to  $l_i$ 's and  $h_i$ 's. We show the optimal solution is that the wire is divided into equal length segments and the widths of the segments form a geometric progression (i.e. for  $1 \leq i \leq n$ ,  $h_i = h_1 \alpha^{i-1}$  for some constants  $h_1$  and  $\alpha$ ).

**Lemma 1** If  $f(x) = Ax + B/x + C$  where  $A > 0$ ,  $B > 0$ , and  $A, B, C$  are independent of  $x$ , then  $f(x)$  is minimum when  $x = \sqrt{B/A}$ .

**Proof:**  $f'(x) = A - B/x^2 = 0 \Rightarrow x = \sqrt{B/A}$ . Also  $f''(\sqrt{B/A}) = 2A\sqrt{A/B} > 0$ .  $\square$

**Lemma 2** If  $f(x) = Ax^2 + Bx + C$  where  $A > 0$ , and  $A, B, C$  are independent of  $x$ , then  $f(x)$  is minimum when  $x = -B/(2A)$ .

**Proof:**  $f'(x) = 2Ax + B = 0 \Rightarrow x = -B/(2A)$ . Also  $f''(x) = 2A > 0$ .  $\square$

For any segment, the *upstream resistance* is the sum of all resistances from the driver (or the last buffer before the segment) to the segment (excluding the segment). The *downstream capacitance* is the sum of all capacitances from the segment (excluding the segment) to the sink (or the next buffer after the segment).

**Lemma 3** For the optimal solution of WIS, for any  $i$  such that  $1 \leq i \leq n$ ,  $h_i = \sqrt{\frac{r_0 C_D}{c_0 R_U}}$ , where  $R_U$  and  $C_D$  are the upstream resistance and the downstream capacitance of segment  $i$  respectively.

**Proof:**

$$D = R_U(c_0 l_i h_i + C_D) + \frac{r_0 l_i}{h_i} \left( \frac{c_0 l_i h_i}{2} + C_D \right)$$

$$\begin{aligned}
& + \text{terms independent of } h_i \\
& = h_i \cdot R_U c_0 l_i + \frac{1}{h_i} \cdot r_0 C_D l_i + \text{terms independent of } h_i
\end{aligned}$$

By Lemma 1, optimal  $h_i = \sqrt{\frac{r_0 C_D l_i}{R_U c_0 l_i}} = \sqrt{\frac{r_0 C_D}{c_0 R_U}}$ .  $\square$

**Lemma 4** For the optimal solution of WIS,  $h_1 > \dots > h_n$ .

**Proof:** For any  $i$ , the upstream resistance of segment  $i$  is smaller than that of segment  $i+1$  and the downstream capacitance of segment  $i$  is larger than that of segment  $i+1$ . So by Lemma 3,  $h_i > h_{i+1}$ .  $\square$

**Lemma 5** For the optimal solution of WIS,  $l_1 = l_2 = \dots = l_n = L/n$ .

**Proof outline:** Consider segment  $i$  and segment  $i+1$ . Let  $R_U$  be the upstream resistance of segment  $i$  and  $C_D$  be the downstream capacitance of segment  $i+1$ . Note that  $R_U$  and  $C_D$  are independent of  $h_i$ ,  $h_{i+1}$ ,  $l_i$  and  $l_{i+1}$  if  $l_i + l_{i+1}$  is fixed.

$$\begin{aligned}
D & = R_U(c_0 l_i h_i + c_0 l_{i+1} h_{i+1} + C_D) \\
& + \frac{r_0 l_i}{h_i} \left( \frac{c_0 l_i h_i}{2} + c_0 l_{i+1} h_{i+1} + C_D \right) \\
& + \frac{r_0 l_{i+1}}{h_{i+1}} \left( \frac{c_0 l_{i+1} h_{i+1}}{2} + C_D \right) \\
& + \text{terms independent of } h_i, h_{i+1}, l_i \text{ and } l_{i+1} \quad (2)
\end{aligned}$$

By Lemma 3,

$$h_i = \sqrt{\frac{r_0(c_0 l_{i+1} h_{i+1} + C_D)}{c_0 R_U}} \quad (3)$$

$$h_{i+1} = \sqrt{\frac{r_0 C_D}{c_0(R_U + r_0 l_i/h_i)}} \quad (4)$$

Let  $\hat{L} = l_i + l_{i+1}$ . If we substitute  $l_{i+1}$  by  $\hat{L} - l_i$  into (2) and simplify,

$$\begin{aligned}
D & = (r_0 c_0 - r_0 c_0 \frac{h_{i+1}}{h_i}) l_i^2 \\
& + (R_U c_0 h_i - R_U c_0 h_{i+1} + \frac{r_0 c_0 h_{i+1} \hat{L}}{h_i} + \frac{r_0 C_D}{h_i} \\
& \quad - r_0 c_0 \hat{L} - \frac{r_0 C_D}{h_{i+1}}) l_i \\
& + \text{terms independent of } l_i
\end{aligned}$$

By Lemma 4,  $r_0 c_0 - r_0 c_0 h_{i+1}/h_i > 0$ . So by Lemma 2 and after simplification,

$$l_i = \frac{1}{2} \left( \hat{L} + \frac{C_D}{c_0} \frac{1}{h_{i+1}} - \frac{R_U}{r_0} h_i \right) \quad (5)$$

Using (3), (4) and (5) to eliminate  $h_i$  and  $h_{i+1}$ , we can show  $l_i = \hat{L}/2$ . That means  $l_i = l_{i+1} = \hat{L}/2$ . In other words,  $l_1 = l_2 = \dots = l_n = L/n$ .  $\square$

**Lemma 6** For the optimal solution of WIS,  $h_1, h_2, \dots, h_n$  form a geometric progression.

**Proof outline:** Consider segment  $i$ , segment  $i+1$  and segment  $i+2$ . Let  $R_U$  be the upstream resistance of segment  $i$  and  $C_D$  be the downstream capacitance of segment  $i+2$ . Let  $l = L/n$ . By Lemma 5,  $l_i = l_{i+1} = l_{i+2} = l$ . By Lemma 3,

$$h_i = \sqrt{\frac{r_0(c_0 l h_{i+1} + c_0 l h_{i+2} + C_D)}{c_0 R_U}} \quad (6)$$

$$h_{i+1} = \sqrt{\frac{r_0(c_0 l h_{i+2} + C_D)}{c_0(R_U + r_0 l/h_i)}} \quad (7)$$

$$h_{i+2} = \sqrt{\frac{r_0 C_D}{c_0(R_U + r_0 l/h_i + r_0 l/h_{i+1})}} \quad (8)$$

Using (6), (7) and (8) to eliminate  $R_U$  and  $C_D$  and rearranging, we get

$$\frac{h_i^2}{h_{i+1}^2} \frac{h_{i+2}}{h_{i+1}} + \frac{h_i}{h_{i+1}} \frac{h_{i+2}^2}{h_{i+1}^2} + \frac{h_i^2}{h_{i+1}^2} \frac{h_{i+2}^2}{h_{i+1}^2} - 1 - \frac{h_{i+2}}{h_{i+1}} - \frac{h_i}{h_{i+1}} = 0$$

or equivalently,

$$\left( \frac{h_i}{h_{i+1}} \frac{h_{i+2}}{h_{i+1}} - 1 \right) \left( \frac{h_i}{h_{i+1}} + 1 \right) \left( \frac{h_{i+2}}{h_{i+1}} + 1 \right) = 0$$

This implies  $\frac{h_i}{h_{i+1}} \frac{h_{i+2}}{h_{i+1}} = 1$ , or equivalently,  $\frac{h_{i+1}}{h_i} = \frac{h_{i+2}}{h_{i+1}}$ , as  $\frac{h_i}{h_{i+1}} + 1 > 0$  and  $\frac{h_{i+2}}{h_{i+1}} + 1 > 0$ . So  $h_i$ 's form a geometric progression.  $\square$

**Lemma 7** For the optimal solution of WIS, for any  $i$

such that  $1 \leq i \leq n$ ,  $h_i = \sqrt{\frac{r_0 C_L}{c_0 R_D} \frac{1}{\alpha^{n-1}}} \alpha^{i-1}$ , and the delay  $D = \frac{r_0 c_0 L^2}{2n^2} \cdot \frac{n + 2\alpha - n\alpha^2}{(1-\alpha)^2}$ , where  $\alpha$  is the root of

$$f(\alpha) = \frac{L}{n} \sqrt{\frac{r_0 c_0}{R_D C_L}} \alpha^{\frac{n+1}{2}} + \alpha - 1 \text{ between } 0 \text{ and } 1.$$

**Proof outline:** Let  $l = L/n$ . By Lemma 5,  $l_i = l$  for  $1 \leq i \leq n$ . By Lemma 6, we know that  $h_i = h_1 \alpha^{i-1}$ ,  $1 \leq i \leq n$ , for some  $\alpha$ . Note that by Lemma 4,  $0 < \alpha < 1$ . Substituting  $l_i$ 's and  $h_i$ 's into (1) and simplifying,

$$\begin{aligned}
D & = R_D C_L + r_0 c_0 l^2 \frac{n}{2} \\
& + r_0 c_0 l^2 ((n-1)\alpha + (n-2)\alpha^2 + \dots + \alpha^{n-1}) \\
& + R_D c_0 l h_1 (1 + \alpha + \dots + \alpha^{n-1}) \\
& + \frac{r_0 l C_L}{h_1} \left( 1 + \frac{1}{\alpha} + \dots + \frac{1}{\alpha^{n-1}} \right) \quad (9)
\end{aligned}$$

Applying Lemma 1 by viewing (9) as a function of  $h_1$ , and

simplifying, we get  $h_1 = \sqrt{\frac{r_0 C_L}{c_0 R_D} \frac{1}{\alpha^{n-1}}}$ .

Substituting  $h_1$  into (9) and simplifying,

$$\begin{aligned}
D & = R_D C_L + r_0 c_0 l^2 \frac{n}{2} \\
& + r_0 c_0 l^2 \left( \frac{\alpha^{n+1} - n\alpha^2 + (n-1)\alpha}{(1-\alpha)^2} \right) \\
& + 2l \sqrt{r_0 c_0 R_D C_L} \left( \frac{1}{\alpha^{\frac{n-1}{2}}} \cdot \frac{1-\alpha^n}{1-\alpha} \right) \quad (10)
\end{aligned}$$

Differentiating (10) with respect to  $\alpha$  and simplifying, we get

$$\frac{dD}{d\alpha} = l \left( \frac{r_0 c_0 l}{\alpha - 1} + \frac{\sqrt{r_0 c_0 R_D C_L}}{\alpha^{\frac{n+1}{2}}} \right) \cdot \frac{(n-1)\alpha^{n+1} - (n+1)\alpha^n + (n+1)\alpha - (n-1)}{(1-\alpha)^2}$$

We can verify that  $\frac{d^2 D}{d\alpha^2} > 0$ . So

$$\begin{aligned} D \text{ is minimized} &\Leftrightarrow \frac{dD}{d\alpha} = 0 \\ &\Leftrightarrow \frac{r_0 c_0 l}{\alpha - 1} + \frac{\sqrt{r_0 c_0 R_D C_L}}{\alpha^{\frac{n+1}{2}}} = 0 \quad (11) \\ &\Leftrightarrow l \sqrt{\frac{r_0 c_0}{R_D C_L}} \alpha^{\frac{n+1}{2}} + \alpha - 1 = 0 \end{aligned}$$

where line (11) is because  $(n-1)\alpha^{n+1} - (n+1)\alpha^n + (n+1)\alpha - (n-1) < 0$  as  $0 < \alpha < 1$  by Lemma 4.

To find  $D$ , note that  $l \sqrt{\frac{r_0 c_0}{R_D C_L}} \alpha^{\frac{n+1}{2}} + \alpha - 1 = 0$  implies  $\sqrt{R_D C_L} = l \sqrt{r_0 c_0} \alpha^{\frac{n+1}{2}} / (1 - \alpha)$ . Substitute  $\sqrt{R_D C_L}$  into (10) and simplify, we get the expression for  $D$ .  $\square$

By Lemma 4, we know that the optimal value of  $\alpha$  is between 0 and 1. Since  $f(0) < 0 < f(1)$  and  $f'(\alpha) = \frac{L}{n} \sqrt{\frac{r_0 c_0}{R_D C_L}} \cdot \frac{n+1}{2} \alpha^{\frac{n-1}{2}} + 1 > 0$  for  $0 < \alpha < 1$ ,  $f(\alpha)$  has a unique root in  $0 < \alpha < 1$ , which can be easily found by bisection method for example.

The results of Lemma 5 and Lemma 7 can be summarized by the following theorem:

**Theorem 1** *For the optimal solution of the wire sizing problem (WIS), we have*

$$\begin{aligned} l_i &= L/n \quad \text{for } 1 \leq i \leq n \\ h_i &= \sqrt{\frac{r_0 C_L}{c_0 R_D} \frac{1}{\alpha^{n-1}} \alpha^{i-1}} \quad \text{for } 1 \leq i \leq n \\ D &= \frac{r_0 c_0 L^2}{2n^2} \cdot \frac{n+2\alpha - n\alpha^2}{(1-\alpha)^2} \end{aligned}$$

where  $\alpha$  is the root of  $f(\alpha) = \frac{L}{n} \sqrt{\frac{r_0 c_0}{R_D C_L}} \alpha^{\frac{n+1}{2}} + \alpha - 1$  between 0 and 1.

**Remark:** A continuous version of the wire sizing problem has been considered in [2] and [11]. That is the optimal continuous function that describes the shape of a wire is given in these two papers. Note that our result here is more general as Theorem 1 implies their results when  $n$  tends to infinity.

### 3. SIMULTANEOUS BUFFER INSERTION/SIZING AND WIRE SIZING WITH $m$ BUFFERS

For convenience, in the rest of the paper, we will treat the driver and the load as buffers of fixed size. We will call the driver the 0th buffer and the load the  $(m+1)$ th buffer. Let  $b_0 = r_g/R_D$  and  $b_{m+1} = C_L/c_g$ . For  $0 \leq j \leq m+1$ , let

$s_j = n_0 + \dots + n_{j-1}$ . In other words,  $s_j$  is the total number of segments between the driver and the  $j$ th buffers.

In this section, we consider the simultaneous buffer insertion/sizing and wire sizing problem with  $m$  buffers (i.e. BISWIS/ $m$ ). Therefore, we minimize  $D$  over  $n_0, \dots, n_m, b_1, \dots, b_m, l_1, \dots, l_n$  and  $h_1, \dots, h_n$ . However, we will first consider a restricted version of BISWIS/ $m$  such that  $m$  as well as  $n_0, \dots, n_m$  are fixed (with  $n_0 + \dots + n_m = n$ ). Note that if we consider the piece of wire between the  $j$ th buffer and the  $(j+1)$ th buffer, the sizing problem of it is similar to the one discussed in Section 2 with  $n_j$  segments. However, the upstream resistance, which is  $r_g/b_j$ , and the downstream capacitance, which is  $c_g b_{j+1}$ , and the length of this piece are not fixed as we allow variables to be changed simultaneously. This complicates the problem a lot. In what follows, we exploit some interesting properties of the optimal solution so that the problem can be handled.

**Lemma 8** *For the optimal solution of BISWIS/ $m$  with  $n_0, \dots, n_m$  fixed,  $l_1 = l_2 = \dots = l_n = L/n$ .*

**Proof outline:** For any  $j$ , consider the  $j$ th buffer, segment  $s_j$  and segment  $s_j + 1$  (i.e. the 2 segments around the  $j$ th buffer). Let  $R_U$  be the upstream resistance of segment  $s_j$  and  $C_D$  be the downstream capacitance of segment  $s_j + 1$ . Note that  $R_U$  and  $C_D$  are independent of  $b_j, h_{s_j}, h_{s_j+1}, l_{s_j}$  and  $l_{s_j+1}$  if  $l_{s_j} + l_{s_j+1}$  is fixed.

If we write  $D$  as a function of  $h_{s_j}$  and  $h_{s_j+1}$ , use Lemma 3 to find  $h_{s_j}$  and  $h_{s_j+1}$ , and then put them back to  $D$  and simplify, we get

$$\begin{aligned} D &= \frac{r_0 c_0 l_{s_j}^2}{2} + 2l_{s_j} \sqrt{r_0 c_0 R_U (c_g b_j)} + R_U (c_g b_j) \\ &+ \frac{r_0 c_0 l_{s_j+1}^2}{2} + 2l_{s_j+1} \sqrt{r_0 c_0 C_D \frac{r_g}{b_j}} + C_D \frac{r_g}{b_j} + D' \end{aligned}$$

where  $D'$  are terms independent of  $b_j, h_{s_j}, h_{s_j+1}, l_{s_j}$  and  $l_{s_j+1}$ . Putting  $l_{s_j+1} = \hat{L} - l_{s_j}$  into  $D$  and let  $\rho = \sqrt{r_0 c_0 r_g c_g}$ , we can write

$$\begin{aligned} D &= r_0 c_0 l_{s_j}^2 \\ &+ \left( 2\rho \sqrt{\frac{b_j}{r_g/R_U}} - 2\rho \sqrt{\frac{C_D/c_g}{b_j}} - r_0 c_0 \hat{L} \right) l_{s_j} \\ &+ \left( \frac{r_0 c_0 \hat{L}^2}{2} + 2\hat{L} \rho \sqrt{\frac{C_D/c_g}{b_j}} \right. \\ &\quad \left. + r_g c_g \left( \frac{b_j}{r_g/R_U} + \frac{C_D/c_g}{b_j} \right) + D' \right) \end{aligned}$$

This is a quadratic equation in  $l_{s_j}$ . By Lemma 2,  $D$  is minimized when

$$l_{s_j} = - \frac{2\rho \sqrt{\frac{b_j}{r_g/R_U}} - 2\rho \sqrt{\frac{C_D/c_g}{b_j}} - r_0 c_0 \hat{L}}{2r_0 c_0} \quad (12)$$

Substituting  $l_{s_j}$  back to  $D$  and simplifying, we get

$$\begin{aligned} D &= \frac{r_0 c_0 \hat{L}^2}{4} + \rho \left( \sqrt{\frac{b_j}{r_g/R_U}} + \sqrt{\frac{C_D/c_g}{b_j}} \right) \hat{L} \\ &+ 2\sqrt{r_g c_g R_U C_D} + D' \end{aligned}$$

Consider  $D$  as a function of  $\sqrt{b_j}$ . By Lemma 1,  $D$  is minimized when  $b_j = \sqrt{C_D/c_g} / (1/\sqrt{r_g/R_U})$ . Put  $b_j$  into (12)

and simplify, we can show  $l_{s_j} = \hat{L}/2$ . So  $l_{s_{j+1}} = l_{s_j}$ . This together with Lemma 5 implies  $l_1 = l_2 = \dots = l_n = L/n$ .  $\square$

By Lemma 6, we know  $h_{s_{j+1}}, h_{s_{j+2}}, \dots, h_{s_{(j+1)}}$  form a geometric progression for each  $0 \leq j \leq m$ . Let  $\alpha_j$  be the constant such that  $h_{s_{j+i}} = h_{s_{j+1}} \alpha_j^{i-1}$  for  $1 \leq i \leq n_j$ .

**Lemma 9** For the optimal solution of BISWIS/ $m$  with  $n_0, \dots, n_m$  fixed,  $\alpha_0 = \alpha_1 = \dots = \alpha_m$ .

**Proof outline:** Let  $l = L/n$ . By Lemma 8,  $l_i = l$  for all  $i$ .

Note that if  $b_1, \dots, b_m$  are fixed, the sizing of the piece of wire between two adjacent buffers is basically an instance of

WIS. So by Theorem 1,  $l \sqrt{\frac{r_0 c_0 b_{j-1}}{r_g c_g b_j} \alpha_j^{\frac{n_{j-1}+1}{2}}} + \alpha_{j-1} - 1 = 0$

and  $l \sqrt{\frac{r_0 c_0 b_j}{r_g c_g b_{j+1}} \alpha_j^{\frac{n_j+1}{2}}} + \alpha_j - 1 = 0$ . Note that  $\alpha_{j-1}$  and  $\alpha_j$  are functions of  $b_j$  but  $\alpha_{j'}$  is independent of  $b_j$  for all

$j' \neq j-1, j$ . Let  $D_j = \frac{r_0 c_0 l^2 n_j + 2\alpha_j - n_j \alpha_j^2}{2(1-\alpha_j)^2}$ . Then by

Theorem 1,  $D = m r_g c_d + \sum_{j=0}^m D_j$ . Note that only  $D_{j-1}$  and

$D_j$  are dependent on  $b_j$ . Differentiate  $D$  with respect to  $b_j$  and after a lot of simplification,

$$\frac{dD}{db_j} = \frac{r_0 c_0 l^2}{b_j} \left( \frac{\alpha_{j-1}}{(1-\alpha_{j-1})^2} - \frac{\alpha_j}{(1-\alpha_j)^2} \right)$$

We can verify that  $\frac{d^2 D}{db_j^2} > 0$ . So

$$\begin{aligned} D \text{ is minimized} &\Leftrightarrow \frac{dD}{db_j} = 0 \\ &\Leftrightarrow \frac{\alpha_{j-1}}{(1-\alpha_{j-1})^2} = \frac{\alpha_j}{(1-\alpha_j)^2} \\ &\Leftrightarrow \alpha_{j-1} = \alpha_j \quad \text{as } \alpha_{j-1} < 1 \text{ and } \alpha_j < 1. \end{aligned}$$

In other words,  $\alpha_0 = \alpha_1 = \dots = \alpha_m$ .  $\square$

**Lemma 10** For the optimal solution of BISWIS/ $m$  with  $n_0, \dots, n_m$  fixed,  $b_j = S^j \frac{\alpha^{s_j+j}}{(1-\alpha)^{2j}} b_0$  for  $1 \leq j \leq m$ ,

$h_i = \sqrt{\frac{r_0 c_g b_j b_{j+1}}{c_0 r_g} \frac{1}{\alpha^{n_{j-1}}} \alpha^{i-s_{j-1}}}$  for  $1 \leq i \leq n$  and  $j$  being the index s.t.  $s_j + 1 \leq i \leq s_{j+1}$  (i.e. the  $i$ th segment is between the  $j$ th buffer and the  $(j+1)$ th buffer), and the delay

$D = m r_g c_d + \frac{r_0 c_0 L^2}{2n^2} \cdot \frac{n + 2(m+1)\alpha - n\alpha^2}{(1-\alpha)^2}$ , where  $\alpha$  is the

root of  $g(\alpha) = \sqrt{\frac{b_0}{b_{m+1}}} S^{\frac{m+1}{2}} \alpha^{\frac{n+m+1}{2}} - (1-\alpha)^{m+1}$  between

0 and 1, and  $S = \frac{r_0 c_0 L^2}{r_g c_g n^2}$ .

**Proof outline:** By Lemma 9, let  $\alpha_0 = \alpha_1 = \dots = \alpha_m = \alpha$ . Let  $l = L/n$ . Then by Theorem 1, for  $0 \leq j \leq m$ ,

$l \sqrt{\frac{r_0 c_0 b_j}{r_g c_g b_{j+1}} \alpha^{\frac{n_j+1}{2}}} + \alpha - 1 = 0$ , or equivalently,

$$\sqrt{b_{j+1}} = \sqrt{S} \alpha^{\frac{n_j+1}{2}} \sqrt{b_j} \quad (13)$$

By (13), it is not difficult to prove that  $b_j = S^j \frac{\alpha^{s_j+j}}{(1-\alpha)^{2j}} b_0$ .

In particular,  $b_{m+1} = S^{m+1} \frac{\alpha^{s_{m+1}+m+1}}{(1-\alpha)^{2(m+1)}} b_0$ . So  $\alpha$  should be the root of the function  $g(\alpha)$  given above. The results on  $h_1, \dots, h_n$  and  $D$  follow directly from Theorem 1.  $\square$

By Lemma 4, we know that the optimal  $\alpha$  is between 0 and 1. It is easy to check that  $g(0) < 0 < g(1)$  and  $g'(\alpha) > 0$  for  $0 < \alpha < 1$ . So  $g(\alpha)$  has a unique root in  $0 < \alpha < 1$ , which can be easily found by bisection method for example.

Notice for Lemma 10 that the optimal delay  $D$  is independent of  $n_0, \dots, n_m$ . That means we can set  $n_0, \dots, n_m$  arbitrarily (with the constraint that  $n_0 + \dots + n_m = n$ ) without affecting the optimal delay. This observation together with Lemma 8 and Lemma 10 give the following theorem:

**Theorem 2** For the optimal solution of the simultaneous buffer insertion/sizing and wire sizing problem with  $m$  buffers (BISWIS/ $m$ ), we have

$$n_j = \text{an arbitrary non-negative integer, for } 0 \leq j \leq m \text{ (s.t. } n_0 + \dots + n_m = n)$$

$$b_j = S^j \frac{\alpha^{s_j+j}}{(1-\alpha)^{2j}} b_0 \quad \text{for } 1 \leq j \leq m$$

$$l_i = L/n \quad \text{for } 1 \leq i \leq n$$

$$h_i = \sqrt{\frac{r_0 c_g b_j b_{j+1}}{c_0 r_g} \frac{1}{\alpha^{n_{j-1}}} \alpha^{i-s_{j-1}}} \quad \text{for } 1 \leq i \leq n$$

with  $j$  being the index s.t.  $s_j + 1 \leq i \leq s_{j+1}$

$$D = m r_g c_d + \frac{r_0 c_0 L^2}{2n^2} \cdot \frac{n + 2(m+1)\alpha - n\alpha^2}{(1-\alpha)^2}$$

where  $b_0 = \frac{r_g}{R_D}$ ,  $b_{m+1} = \frac{C_L}{c_g}$ ,  $s_j = n_0 + \dots + n_{j-1}$ ,  $\alpha$  is the

root of  $g(\alpha) = \sqrt{\frac{b_0}{b_{m+1}}} S^{\frac{m+1}{2}} \alpha^{\frac{n+m+1}{2}} - (1-\alpha)^{m+1}$  between

0 and 1, and  $S = \frac{r_0 c_0 L^2}{r_g c_g n^2}$ .

#### 4. SIMULTANEOUS BUFFER INSERTION/SIZING AND WIRE SIZING WITH OPTIMAL NUMBER OF BUFFERS

Now, we consider the BISWIS problem. Therefore we minimize  $D$  over  $m, n_0, \dots, n_m, b_1, \dots, b_m, l_1, \dots, l_n$  and  $h_1, \dots, h_n$  simultaneously. (See Figure 1.) The following Theorem gives a closed form optimal solution to BISWIS.

**Theorem 3** For the optimal solution of the simultaneous buffer insertion/sizing and wire sizing problem (BISWIS), we have  $m$  is equal to the better one of  $\lfloor \hat{m} \rfloor$  and  $\lceil \hat{m} \rceil$ ,

where  $\hat{m} = - \left( \ln \frac{r_g c_g x}{R_D C_L} \left( \frac{2x + S - \sqrt{4xS + S^2}}{2x} \right)^n \right) / \ln x$ ,

$\left(\frac{x}{e}\right)^x = e^{cd/c_g}$  and  $S = \frac{r_0 c_0 L^2}{r_g c_g n^2}$ . Moreover, the optimal val-

ues of  $n_0, \dots, n_m, b_1, \dots, b_m, l_1, \dots, l_n, h_1, \dots, h_n$  and  $D$  are the same as in Theorem 2.

**Proof outline:** Consider the solution of  $D$  given in Theorem 2 as a function  $m$ . We can show that  $D''(m) > 0$ . So  $D$  is a convex function with respect to  $m$ . We can minimize  $D$  by solving  $D'(m) = 0$ . The solution is  $\hat{m}$ , which may not be an integer. As  $D(m)$  is a convex function, the integer value that minimizes  $D(m)$  is either  $\lfloor \hat{m} \rfloor$  or  $\lceil \hat{m} \rceil$ .  $\square$

## 5. DISCUSSION

There are several interesting points to make about the theorems in this paper. Firstly, although we consider a more general problem by allowing the lengths of segments to be varied, the optimal solution is always that the wire is divided into equal length segments (no matter how many buffers we use and no matter where we put the buffers). That means using different segment lengths does not have any advantage with respect to delay. For previous papers which consider delay minimization by wire sizing, the problems are usually formulated as changing segment widths while segment lengths are given as input. In [7] and [9], they assume that the input segment lengths are all equal and then they solve the problems by iterative algorithms. Our results justify the assumption they made.

Secondly, we have pointed out that the optimal delay  $D$  is independent of  $n_0, n_1, \dots, n_m$ . That means we can put the buffers anywhere between two adjacent segments without affecting the optimal delay. Although this flexibility is not useful in minimizing delay, it can be used to optimize other objectives such as total wire area, total power consumption or maximum wire width.

We can extend our results to handle nets with tree topology by a similar technique as [4]. That is we use an iterative algorithm to size the tree edges one at a time. At each time we manipulate an edge, we keep the sizes of all the other edges fixed and apply our solution to that edge. This method should be much faster and use much less memory than an iterative algorithm which divides each tree edge into several segments and locally sizes a segment at each step.

The major weakness of our results is probably that we have ignored wire fringing capacitance in our problem formulation. Fringing capacitance will become more important as wires will become narrower. However, the closed form solution is expected to be much more complicated if fringing capacitance is considered. For example, the lengths of segments will no longer be equal and the widths of segments will no longer form a geometric progression in the optimal solution. We have already done some works on the problem with wire fringing capacitance consideration and we hope we will publish them in near future.

In fact, we have done some experiments to see how good our solution approximates the case with fringing capacitance. We fixed the number of buffers and the buffer positions, add half of the total fringing capacitance to  $C_L$  (i.e. set  $C_L$  to  $C_L + c_f L/2$  where  $c_f$  is the unit wire fringing capacitance) and then obtain a sizing solution by Theorem 2. The delay of our solution is compared with that of the optimal solution (obtained by an iterative algorithm). We have used many different sets of parameters and they all show that the delay is only a few percents off the optimal. For example, for  $r_0 = 0.12\Omega$ ,  $c_0 = 0.04fF/\mu m^2$ ,  $c_f = 0.15fF/\mu m$ ,  $r_g = 814\Omega \mu m$ ,  $c_g = 28fF/\mu m$ ,  $c_d = 0.154ps/\Omega/\mu m$ ,  $R_D = 270\Omega$ ,  $C_L = 5pF$ ,  $L = 3000\mu m$ ,  $n = 8$ ,  $m = 3$  and  $n_0 = n_1 = n_2 = n_3 = 2$ , then the delay of our solution is only 6.1% more than the optimal solution. Hence, we can still apply our results to the case with fringing capacitance to obtain a reasonably good solution.

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