1. (32 pts.) In slide 16 of “IC Technology Scaling”, the effects of full scaling of MOS transistor are highlighted. This question considers a more general scaling model in which dimensions ($W$, $L$, $t_{gox}$, $X_j$) are scaled by $1/S$, substrate doping ($N_{SUB}$) is scaled by $S$, and voltages ($V_{DD}$, $V_{TN}$, $V_{TP}$) are scaled by $1/S_V$.

(a) Please describe how each of the parameters below will be scaled as a function of $S$ and $S_V$. Please show the steps of your derivation.
   i. Current per device.
   ii. Gate capacitance.
   iii. Transistor on-resistance.
   iv. Intrinsic gate delay.
   v. Power-dissipation per gate.
   vi. Power-delay product per gate.
   vii. Area per device.
   viii. Power-dissipation density.

(b) Assume $S$ is $\sqrt{2}$. If we want to keep power-dissipation density the same after scaling, what should be the value of $S_V$? How will the intrinsic gate delay and power-dissipation per gate be changed after scaling? Please show your calculations in detail.

(c) Assume $S$ is $\sqrt{2}$. If power-dissipation density is allowed to be increased by 20%, what should be the value of $S_V$? How will the intrinsic gate delay and power-dissipation per gate be changed after scaling? Please show your calculations in detail.

(d) Compare the scaling in part (c) to the one in part (b) in terms of intrinsic gate delay and power-dissipation per gate?

2. (20 pts.) Please the article “Moore’s Law: A Status Report” (Semiconductor Engineering, Apr. 2017) and summarize the main points of the article in at least 150 words.

3. (13 pts.) Sketch a transistor-level schematic for a CMOS compound gate for the function

$$F = \overline{A} \cdot \overline{B} + \overline{C} \cdot (\overline{D} \cdot E)$$

**Hint:** You may need to perform some logic manipulation to transform the function into a certain form before constructing the gate.