EE 501 Lab 3 Differential Amplifier Design

Lab report due on Sep 24th, 2015

Objectives:

1. Design a differential input and single-ended output cascode amplifier.

Tasks:

1. Build a differential input and single-ended amplifier, telescopic amplifier or folded cascode amplifier (if you have taken EE435 or equivalent courses, do folded cascode design) to meet the design specification.
2. Calculate the desired circuit parameters (such as, tail current, gm, and etc.) to meet design specification. You can follow the procedure in Chapter 5.2 of textbook to size and bias all transistors to meet the specification given below.
3. Explore ways to improve DC gain, such as how to properly choose tail current, transistor sizes, and etc.
4. Explore ways to minimize the input referred voltage noise, such as how to properly choose tail current, transistor sizes, and etc.
5. Understand the design trade-offs of gain, GBW, phase margin, input referred noise voltage, current and area consumption, and etc.

Basic Specification Targets:

1. Load capacitor C_L=1pF
2. V_{DD}=2.5V, Vss=-2.5V
3. Peak DC gain >= 35 dB (60dB for telescopic or folded cascode)
4. GBW>=100MHz
5. Slew rate (SR)>=100V/us
6. Input common mode range (ICMR) >=2.5V
7. Phase margin(PM)>=45 °
8. Minimize power

Report:

1. Full schematics and symbol.
2. Theoretically analysis on design parameters to achieve the specifications.
3. Tabulate the following parameters for all your transistors (Vds, Veff, Id, gm, gds, W/L, Cgs, Cdd, and etc.)
4. Summarize the amplifier performance in a table (Current consumption, DC gain, GBW, UGF, PM, ICMR, SR, total area, input referred noise voltage).
5. Plot Gain vs. Frequency and Phase vs. Frequency waveforms, and mark the DC gain, bandwidth, UGF, and phase margin.
6. Plot input referred noise voltage density vs. frequency

All the parameters simulated above are in the open loop setup. However, since op amplifier is always used in feedback loop, it is more suitable to measure the parameters in close-loop form.

Supposing this amplifier is usually used as a unity-gain driver, try to find test-benches for the following parameters.

7. Loop gain, phase margin and gain margin of the amplifier.
8. Plot ICMR results.
9. Transient simulation results for Slew rate, overshoot and settling time with marker on them. Calculate the value,

   phase margin+overshoot percentage

   For instance, 45+30=75.
10. Description of the design trade-offs, such as how the tail current and input transistor sizes affects the gain, GBW, ICMR, slew rate, noise, and etc,.

Suggestions:

1. Folded-cascode amplifier (example)

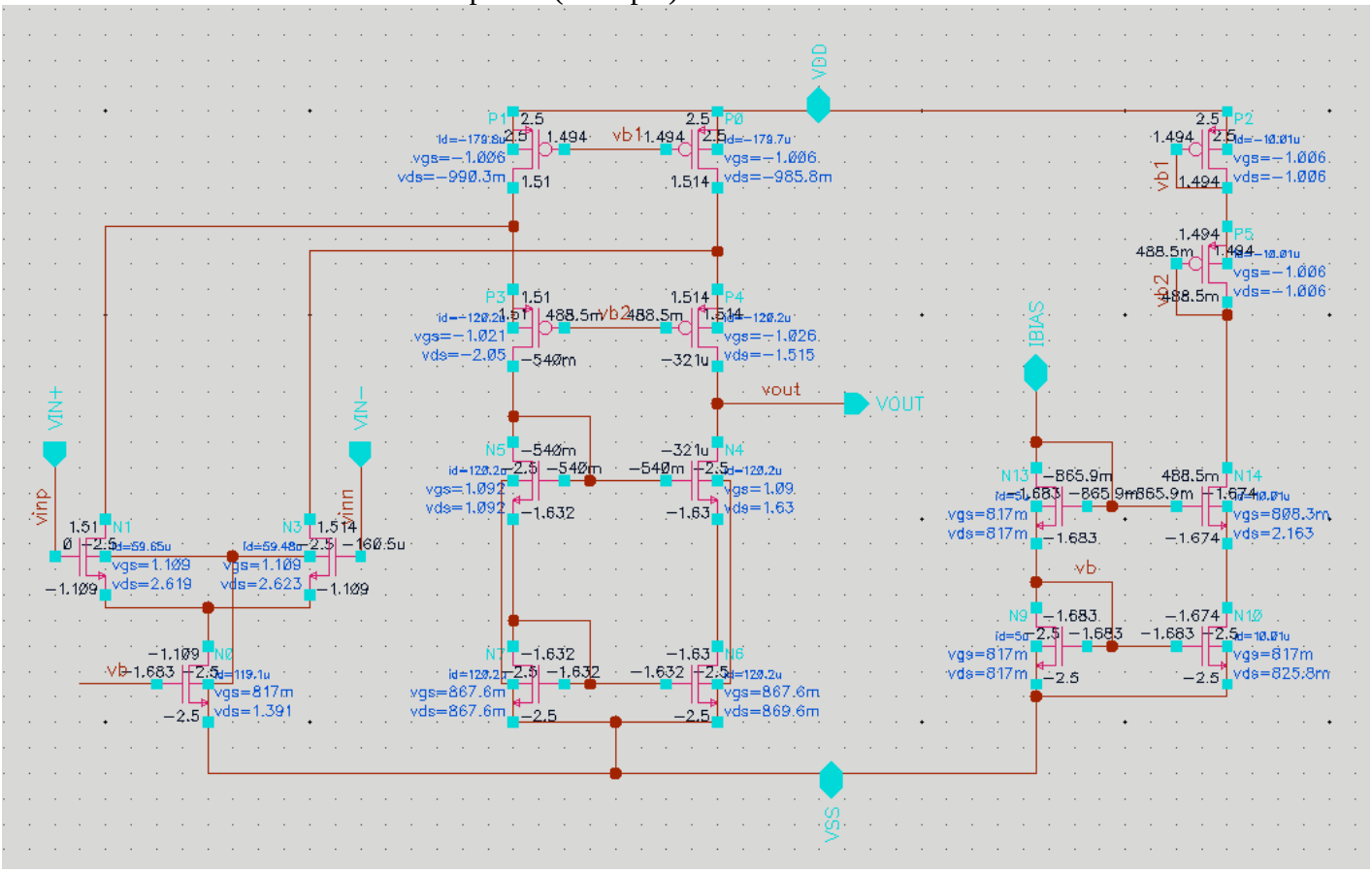

Fig. 1 Folded-cascode amplifier example

2. A symbol of the amplifier is created for being used in test-bench.
   a. Add pins to the input, output and power supplies (“p” for keyboard shortcut).
   b. In the schematic window, click on “create”->“Cellview”->”From Cellview…”

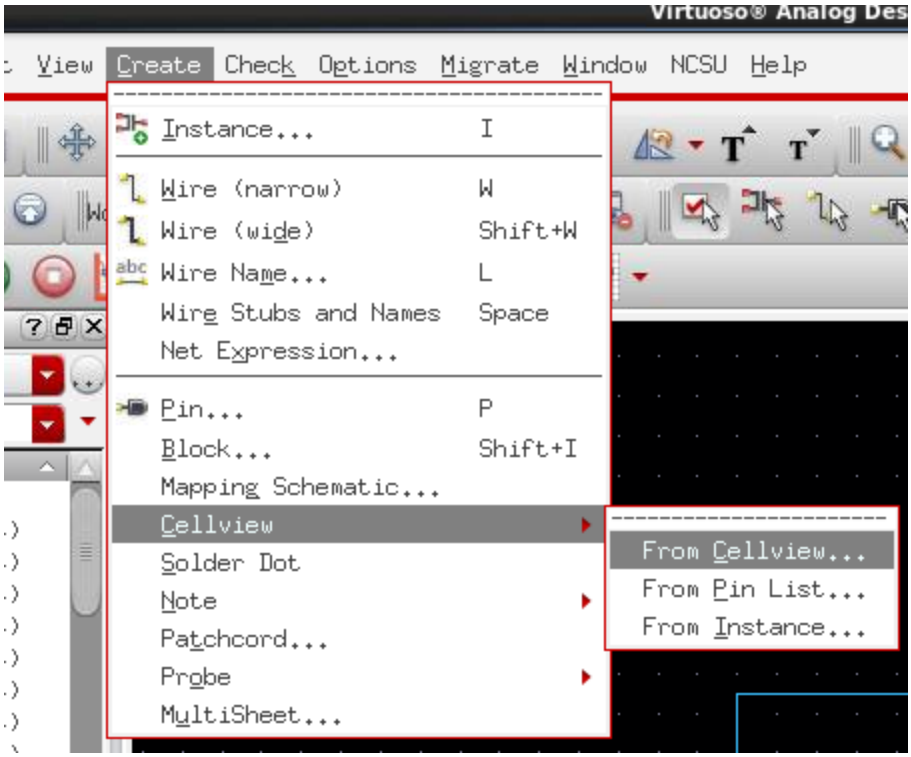

Fig. 2 Symbol creation

c. Click OK and arrange pins.
d. You can redraw your amplifier with a triangle in the symbol cellview.

3. Open loop AC response can be used to help design but it is not the most suitable way to indicate the frequency characteristics of the amplifier. Since the amplifier is always used in feedback loop, the loop gain will finally indicate the stability of the amplifier. Loop gain is often measured in close-loop form. In the loop gain test, "stb" simulation can be used. Test-bench is shown in Fig. 3.
   a. Add a parallel capacitor over the feedback resistor to cancel the effect of amplifier's input capacitance.
   b. The feedback network should have input impedance much larger than your amplifier's output impedance to avoid loading effect and degrading DC gain.
   c. The resistors used in feedback network may be in the order of several mega ohms which is not always the case. This is because the amplifier you are designing has an output structure of cascode which will significantly increase the output impedance. For the future project, it is better to choose reasonable resistor with tens or hundreds kilo ohms.
   d. Insert "vdc" or "iprobe" into the loop where the loop is expected to be broken. You can try different places.
   e. Open the "Analog Design Environment" and choose "stb" simulation.
   f. In "Sweep Range", choose the frequency region from 1 to 10GHz, and select the "vdc" or "iprobe" as "Probe Instance". Setup is shown Fig. 4.
   g. To show the results, in the "Analog Design Environment", choose "Results"->"Direct Plot"->"Main Form…". In the new window, choose "stb" and you can see the stability summaries. This is shown in Fig. 5.

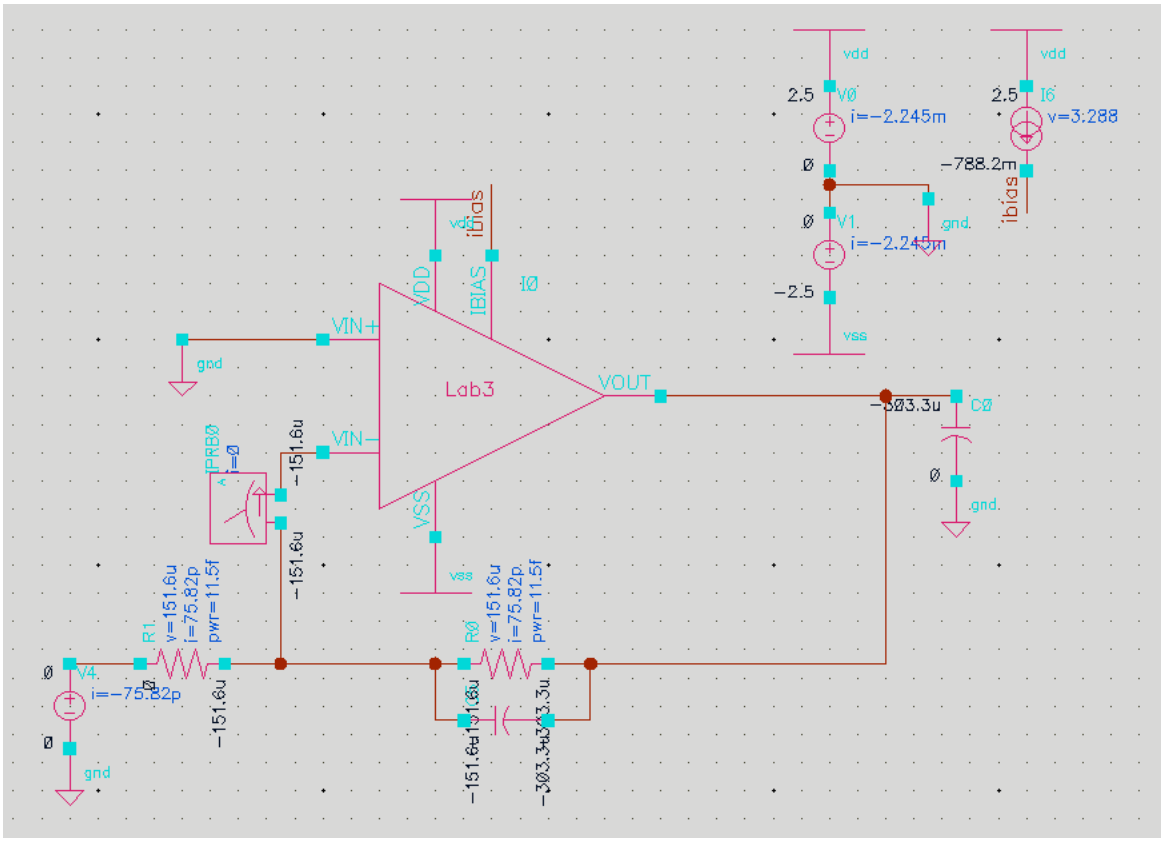

Fig. 3 Loop gain measurement test-bench in close-loop

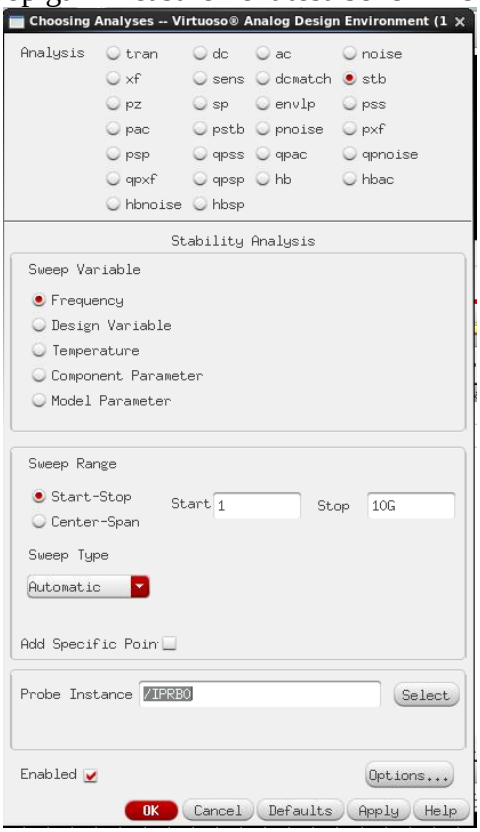

Fig. 4. “stb” simulation setup

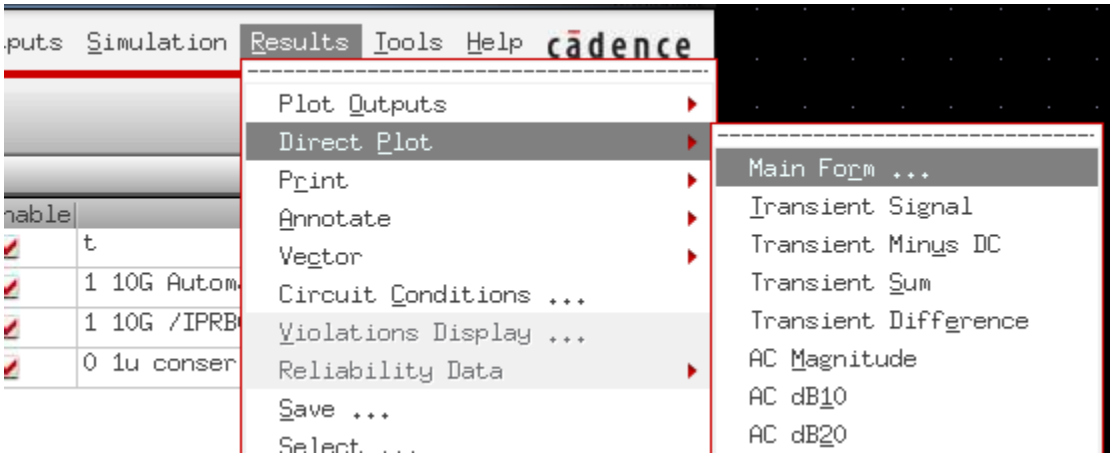

Fig. 5. "stb" results

h. Reference: https://secure.engr.oregonstate.edu/wiki/ams/index.php/Spectre/STB

4. ICMR simulation setup:

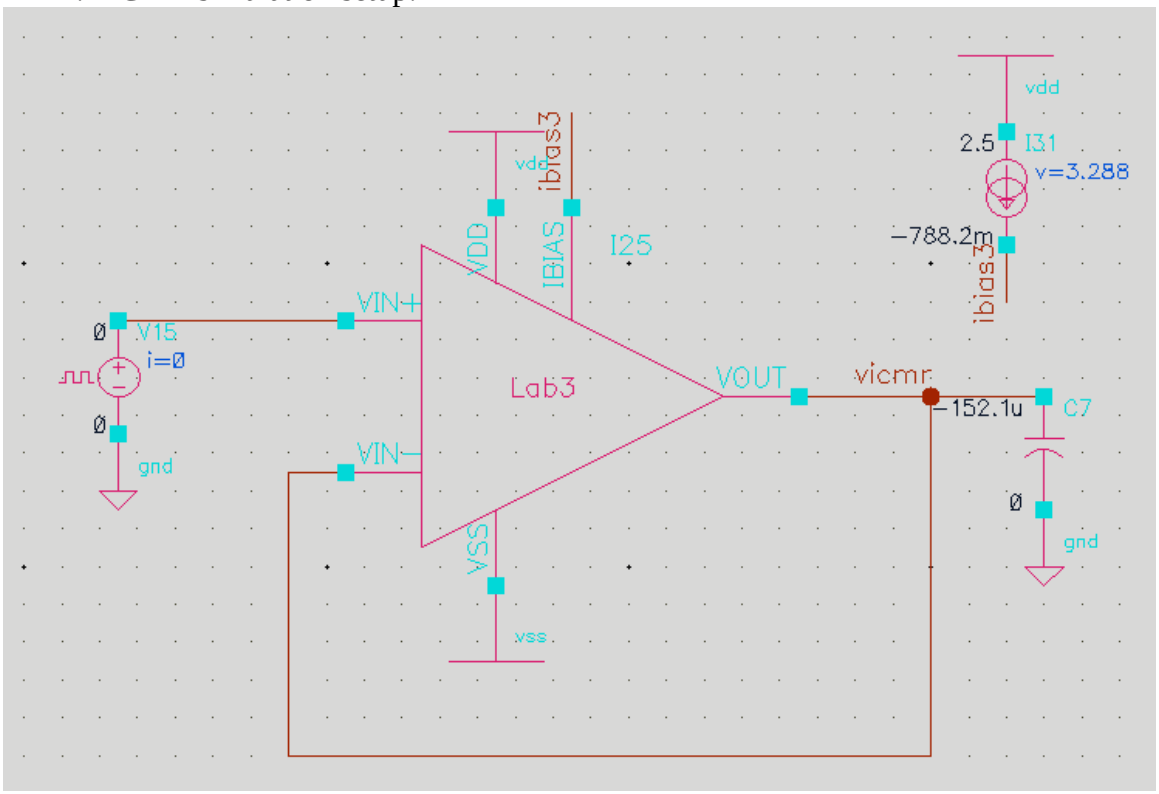

Fig. 6 ICMR simulation setup

a. Connect the amplifier as a unity-gain driver.
b. Parametric sweep the DC parameter of input voltage source ("/V15" in the circuit).
c. Show the waveform of the output node's DC voltage.
d. The linear part of the transfer curve where the slop is unity corresponds to the input common-mode voltage range.

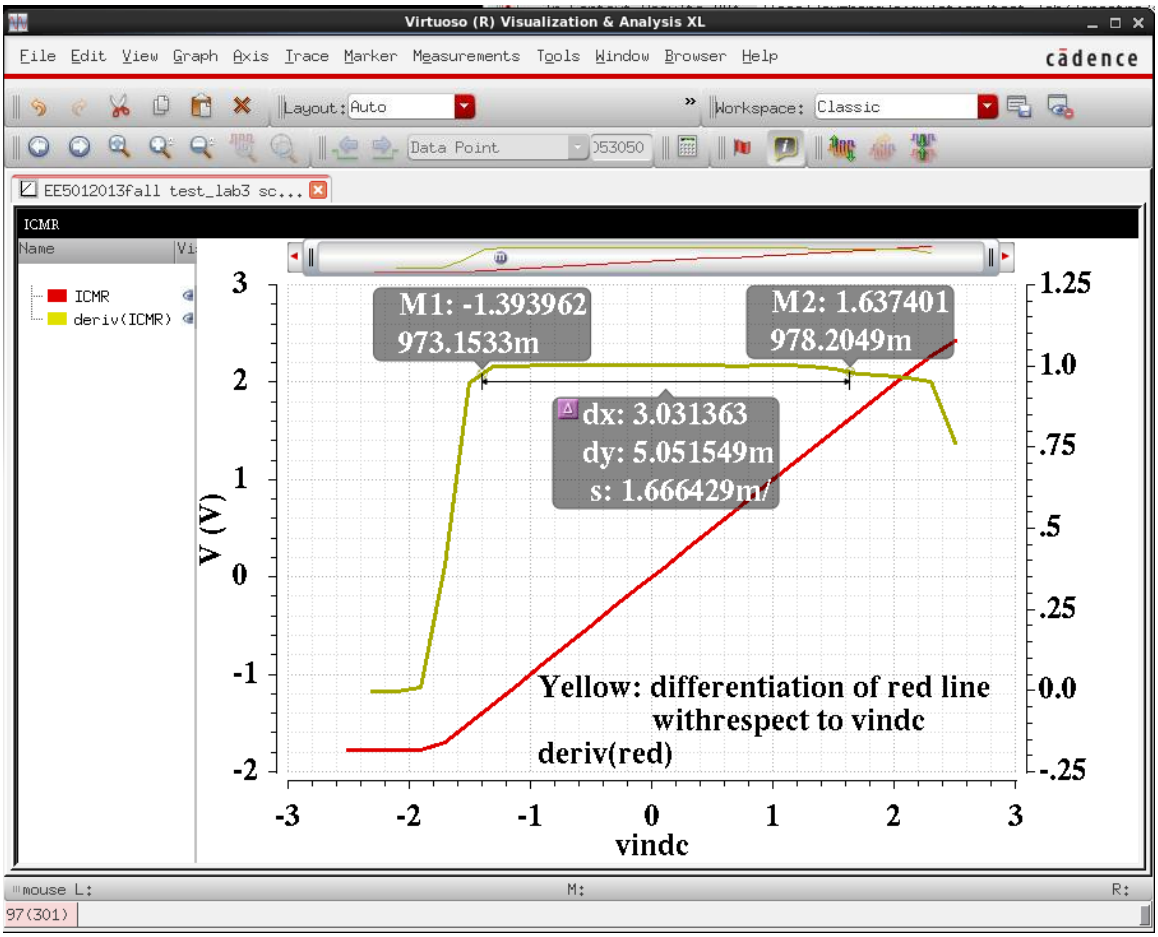

Fig. 7 ICMR of the designed amplifier

5. Slew Rate & Transient Response simulation setup:
   a. Connect the amplifier as a unity-gain driver.
   b. Add a voltage pulse source “vpulse” to stimulate the circuit.
   c. It is better to separate the slew rate and settling time tests. Slew rate is a large signal characteristic and a sufficient large step voltage input is needed (always >0.5V and in this case you can use 1V). If the step is small (<0.5V and you can use 0.1V), the transient response will be a linear response.
   d. In this case, you can set the Rise/Fall time of the pulse as 1ps which can work like an ideal step signal for this amplifier.

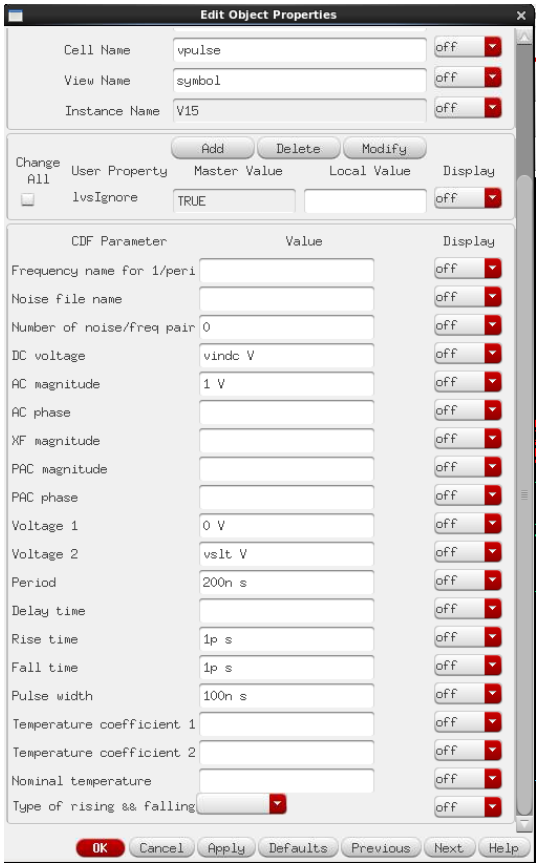

Fig. 8 “vpulse” setup for slew rate and overshoot simulations

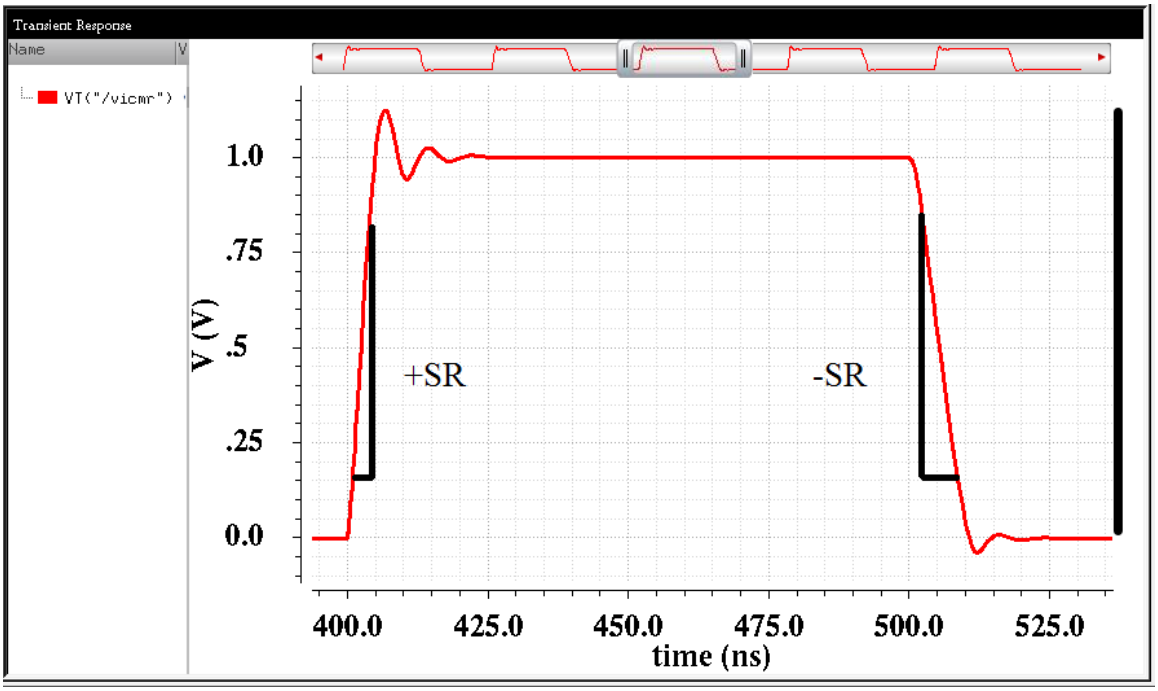

Fig. 9 Slew Rate simulation results

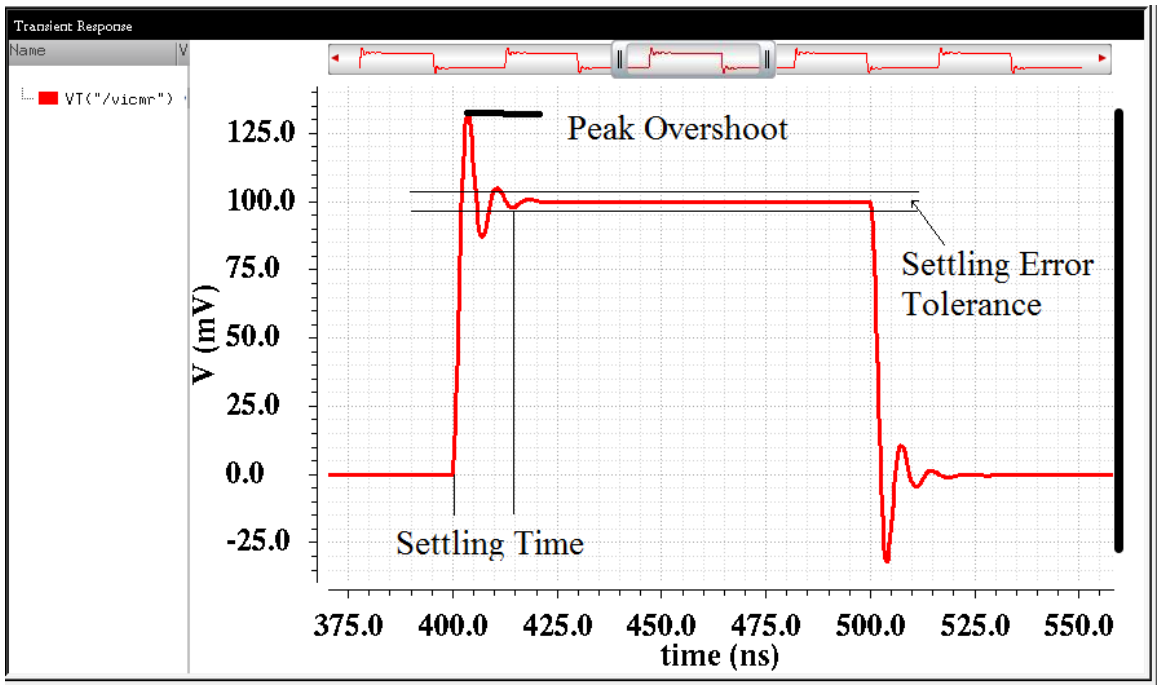

Fig. 10 Overshoot and settling time simulation results

6. Input referred voltage noise

To simulate input referred voltage noise, select noise analysis, set up the following,

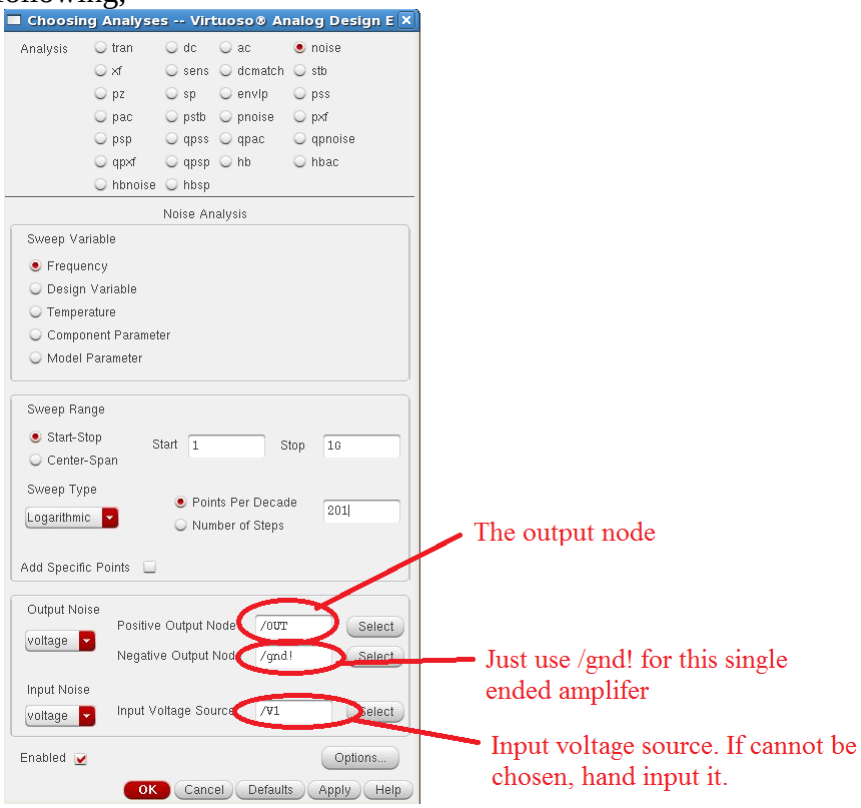

Fig. 11 “noise” simulation setup

After run the simulation you can evaluate your input referred noise from “Result”-> “Direct Plot”->“equivalent input noise”
Use calculator to calculate the average input referred voltage noise density or input referred voltage noise level.

You may inspect the noise contributions of each components from the “noise summery Results”->“Print”->“Noise summary”

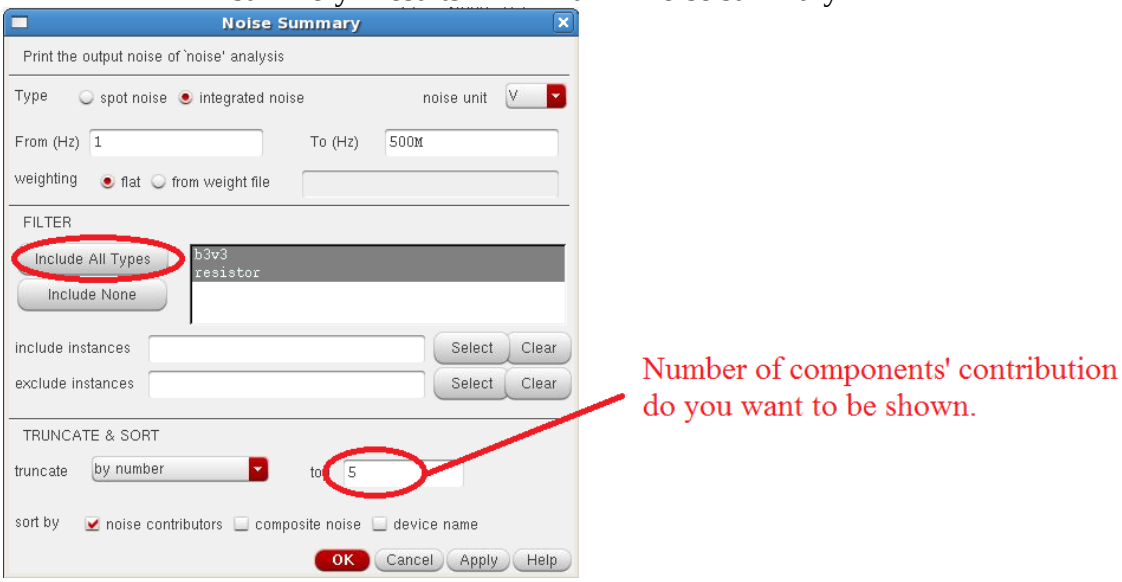

Fig. 12 Showing noise results